General Electric Instrumentation
228 W. Florence
Inglewood, Calif. 90301

Electronic Services - Los Angele
M14731X

PULSECOM

INSTRUCTION MANUAL

Solid State Selector
Model 431-10

IN# 176

(5/70)

Pulse Communications, Inc.
5714 Columbia Pike
Falls Church, Virginia 22041
Telephone: (703) 820-0652
Telex: 89-9423

Digitized by the Internet Archive
in 2025

https://archive.org/details/manualsplus_11216

ADDENDUM B

The following tables list the specific functions of the input/output pins when a Model 431-10 is installed in a Type B station (35ASR split operation). Figure B-1 is an isolated contact diagram of a B type station. Figure B-2 is an isolated-contact relay logic diagram.

Table B-1, Pin Functions

Pin No.	Color	Function
P1-A-5	Yellow	T.D. Contacts
-6	Orange	T.D. Contacts
-8	Black	Punch Blind
-9	Violet	Punch Blind
-10	Grey	
-11	White	R. O. S.M.D.
-12	Red	R.O. S.M.D.
-13	Green	Low Paper Switch
-14	Brown	T.T., T.D. Switch
-15	Blue	GRD.
P2-1	Black	Off Line SW.
-2	Red	Off Line SW.
-3	Orange	Alarm Light
-4	Green	GRD
-5	Blue	Distortion Light
-6	White	BID Light
-7	White/Black	TD ON/OFF Line SW.
-8	Black/White	Off Line CDC Buzzer
-9	Any	Off Line CDC Reset
-10	As Above	Off Line CDC Reset
-11	Orange/Black	None
-12	Green/Black	6.3 VAC Return

Table B-1 (Continued)

Pin No.	Color	Function
P2-13	Green/White	Off Line SW.
-14	Any	CDC Off-Line Reset
-15	As Above	CDC Off-Line Reset
JS3-1	Brown	Clutch
-2	Orange	Clutch
-3	No connection (N.C.)	
-4	Black	Printer Motor
-5	Red	Printer Motor
-6	N.C.	
-7	Green	TD Motor
-8	White	TD Motor
-9	N.C.	
-10	N,C.	
-11	N.C.	
-12	Any	
-13	As Above	
-14	Blue	Off Line Relay in 35
-15	Yellow	Off Line Relay in 35

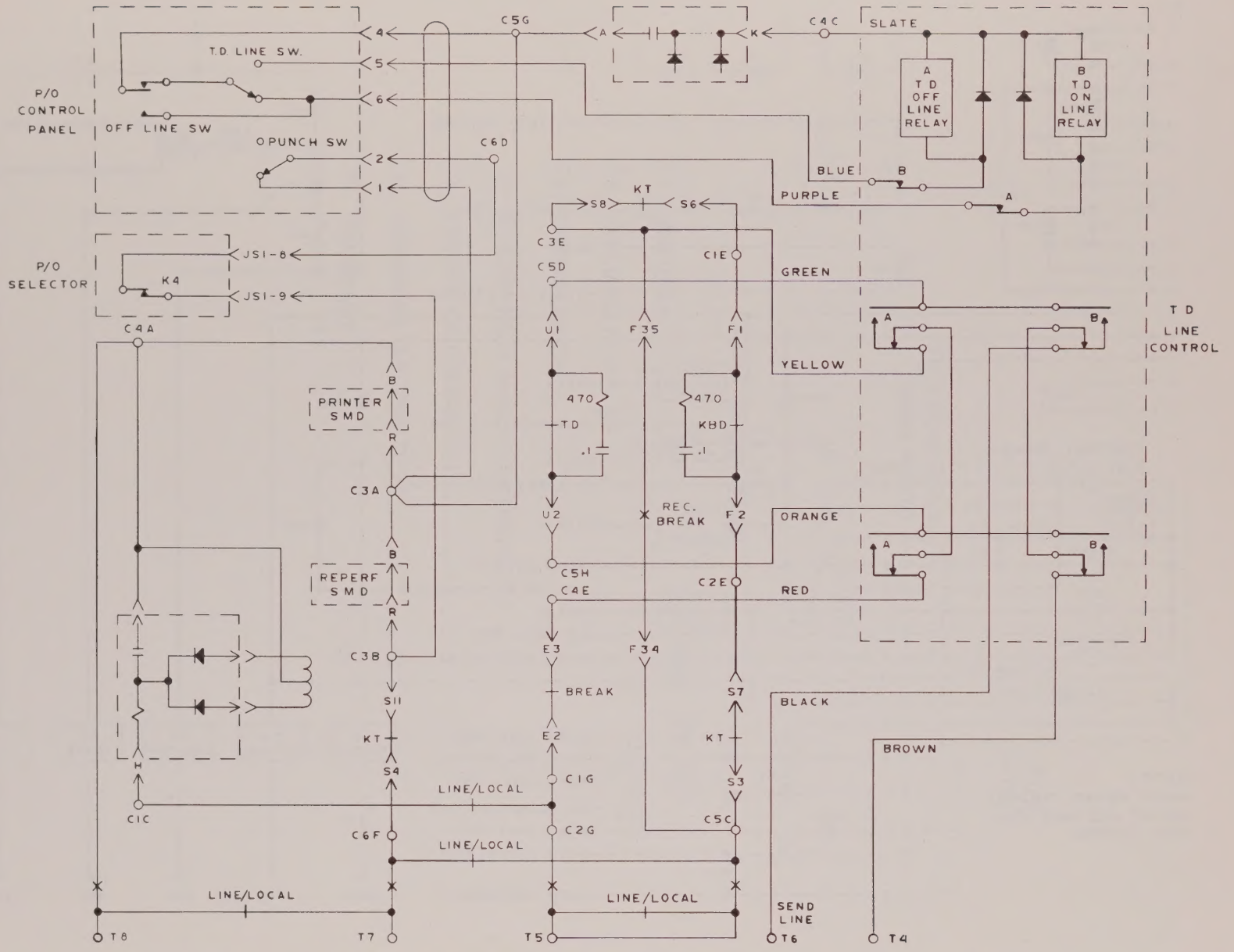


Fig B-1. Isolated Relay Contact Logic Diagram

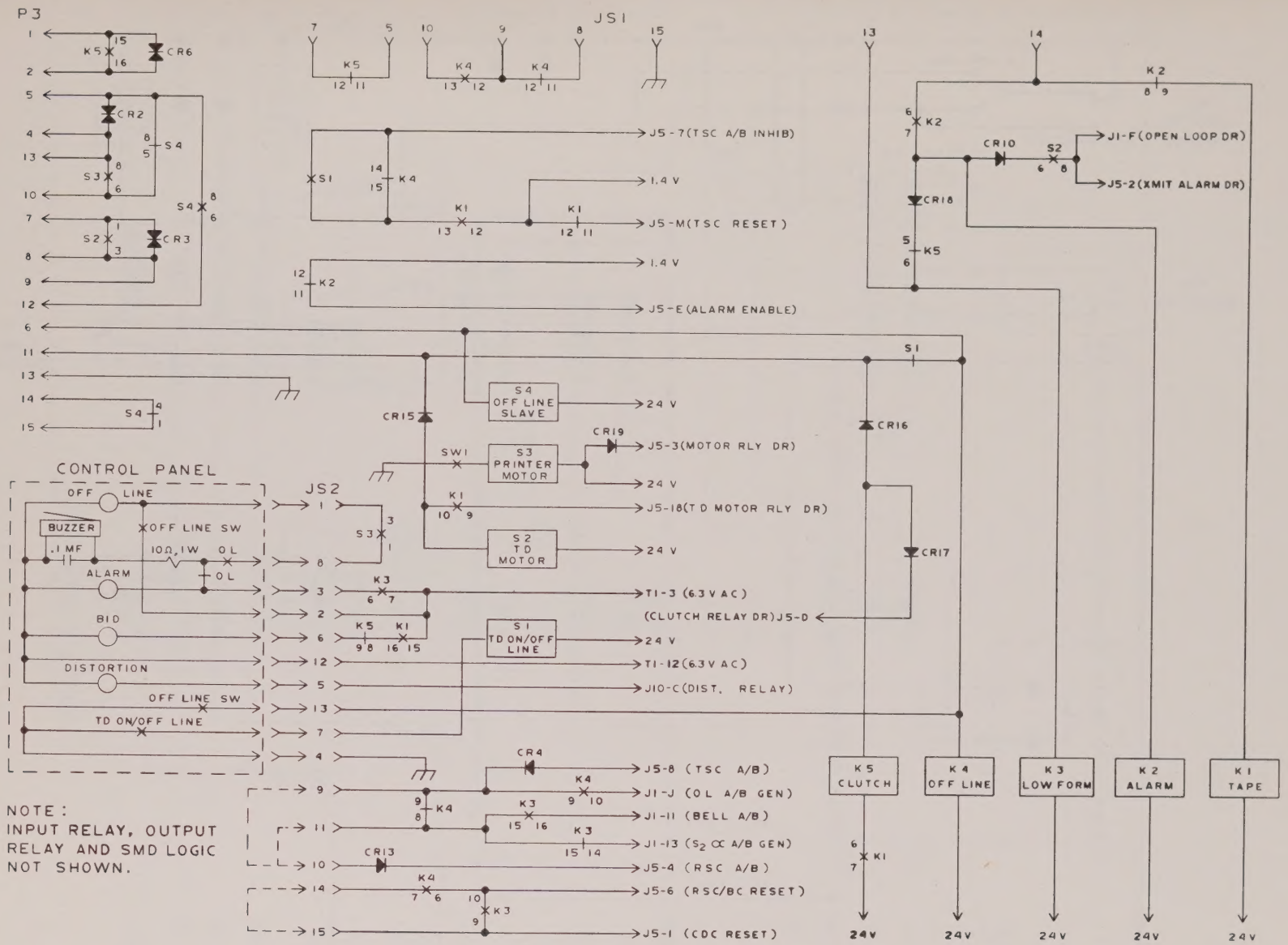


Fig B-2. Isolated Relay Logic Diagram.

IN#176
(5/70)

Solid State Selector
Model 431-10

TABLE OF CONTENTS

	Page
1. GENERAL	1
2. SPECIFICATIONS	1
3. INSTALLATION	3
4. CALIBRATION AND ADJUSTMENTS	4
5. THEORY OF OPERATION	5
6. ORDERING INFORMATION	10
7. DRAWINGS	10

SOLID STATE SELECTOR
Model 431-10

1. GENERAL

The 431-10 is an assembly of Pulsecom's Solid State Selector building blocks. It provides all the character sequence recognition and control necessary to interface an M33 or M35 Teletype with a modified 8A1 or 8B1 telegraph line using 63 ASCII or can be modified to many other formats. It can be operated in full or half-duplex. All communication is to and from the processor - no intra-line calling. The parity-checking option checks all incoming characters for correct parity (even). If the parity is wrong, the selector substitutes a "flag" character in the copy. This does not destroy the character following misparity.

2. SPECIFICATIONS

Code Sequences Recognized

Transmitter Start Code (TSC): $DC_0\alpha$
Receiver Start Code (RSC): Sometimes called a CDC: $S_1\alpha$
Full Duplex Interrupt:
(1) Temporary Inhibit (TI): S_0DEL
(2) Resume Transmission (RTX): Single character, EOA.
Release Code (SOT): Single character, SOT
Full Duplex Tape Stop: Interrupt (S_0DEL) followed by X-OFF

Station Responses

1. To Transmitter Start Code ($DC_0\alpha$)
   a) If tape and station are ready to send:
      1) Motor starts
      2) After about 1 second, the tape starts through the reader and continues until the selector stops it or the tape runs out or becomes tight.
   b) If station is not ready to send:
      1) No Traffic Answerback: $S_2\alpha$
2. To Receiver Start Code ($S_1\alpha$)
   a) Station ready to receive:
      1) Motor starts
      2) Selector Sends on-line answerback: $S_2\alpha$
      3) Station printer ready to copy when SOT is received
   b) Low paper condition in existance at station:
      1) Send low paper A/B (Bell)
   c) Station off-Line
      1) Send off-line answerback: FE_0

3. To End of Address Code (EOA)
   a) Blind selector to further receipt of RSC (or TSC's in FDX) until recognition of EOT
   b) If station selected, gate following signals to receive printer
   c) Release station from standby status if placed there by Interrupt
4. To End of Transmit Code (EOT)
   a) If printing a receive message, stop
   b) If in half duplex, stop sending
   c) In full duplex the tape will continue
   d) Prepare selector to recognize RSC's (and TSC's if in half duplex)
5. To Full Duplex Interrupt (S_o):
   a) Stop transmitter if transmitting and place in standby
   b) Stop receiver if receiving and place in standby
   c) S_o is followed by delete
   d) Permit selector to recognize TSC or RSC
6. To Full Duplex Resume (EOA)
   a) Allows stations in standby to resume
7. To Full Duplex Tape Stop (S_o DEL X-OFF)
   a) If sending, tape stops on S_o then stops permanently upon recognition of X-OFF A TSC is required to start the tape again
8. To Open Line
   a) If sending - stop tape, light alarm lamp and operate buzzer
   b) If receiving, place mark current to printer magnet, light alarm lamp and operate buzzer. When line closes return printer to the print mode.
   c) If neither sending or receiving, light lamp, operate buzzer
9. To Distortion: When distortion in the incoming signals exceeds 25% an alarm lamp (on the control panel) will light momentarily, then it will reset. If the distortion continues, the lamp will repeatedly turn on then reset itself. This feature permits the operator to determine whether poor terminal performance is because of a defective terminal or defective signals are bing delivered to the terminal.
10. To Misparity, Optional. When an incoming character does not have even parity (zero, two, four, six or eight bits marking) the selector will substitute a "flag" character in place of the misparity. This requires that there be a one character buffer in the selector causing the printer when selected to be one full character behind the signals on the line. Characters only reach the output register after the station has been selected. Once a character is loaded into the output register, it is clocked out to the printer. This allows the turn-off codes to reach the printer.

Control Panel

A Control panel Model 6006-2 is provided with the 431 and mounts in the cutout panel to the right of the M33 or M35 Teletype machines. It contains the following functions:

Bid Lamp, Green. Lights when tape is ready to send

Alarm Lamp, Red. Lights for the duration of: Open line, Low paper

Off-Line Lamp, Orange. Lights when machine is switched off line for preparing tape.

Distortion Lamp, Blue. Lights momentarily for each detection of distortion above threshold.

On-Line/Off-Line Switch. When off line, the selector:

a) Light the Off-Line, Lamp,
b) Conditions the selector to respond to an RSC with the Off-Line answerback, FE_o,
c) Transfers the machine keyboard, printer and tape punch to its local loop.
d) Conditions the buzzer to operate momentarily upon recognition of an RSC.

Buzzer. The buzzer operates momentarily when an RSC is recognized and the machine is off-line. It will operate whenever the alarm lamp is lit but is resetable by operating the off-line switch to off, then on.

Telegraph Interface

Code: 8-level USASCII

Loop Current: 20-60 ma polar or neutral strap adjustment on bias of input relay

Input Impedance: 36-ohm coil of input relay (mercury-wetted contacts) - or EIA RS-232

Output to Loop: Contacts of send relay are mercury wetted and spark-suppressed. They are the only contacts in the transmission path. If either the receive or send loop opens elsewhere, or power is lost to the selector, the send relay will remain closed or EIA RS-232.

Acceptable Input Distortion: 42%

Output Distortion (to loop or printer): Less than 3% average, 6% maximum

Speed: Adjustable between 66 and 150 baud, may be present at factory or set in the field. Adjustments should be made with the aid of an electronic counter. Field adjustments are possible with a volt meter and satisfactory source of incoming signals.

Other Characteristics

Motor Control: Keeps motors off except on RSC's or TSC when tape is to be sent. There is a 0.6 sec delay before triggering the on-line answerback to permit the motor to reach full speed.

Alarm Lamp: For duration of alarm (low paper or open)

Size: 16 in. x -3/4 in. (WxDxH)

Power: 120 v or 230 v ± 10%, 50/60 Hz, 3/8 amp

3. INSTALLATION

This Model 431 Selector is a universal unit that can be used to control several types of stations. The three connectors mounted on the side of the unit are used to carry signals and controls between the selector and the station. The information in this section is for reference purposes only and is only typical. Detailed functions for particular uses are appended to this manual as required.

Socket JS1 is used for signals to the loop and for certain signals to and from the station. The typical functions of the JS1 connectors are:

JS-1	Signal to loop
-2	Signal to loop
-3	Output (answerback) relay control N/C
-4	Output (answerback) relay control C
-5	Output (answerback) relay control N/O - Also TD contact when station operates EIA
-6	TD contact
-7	
-8	
-9	
-10	
-11	Selector magnet drive
-12	Selector magnet drive return
-13	Low paper switch
-14	Tape out switch
-15	Chassis ground

Socket JS2 is used for inter-connections to the control panel. The functions of JS2 are listed on drawing D200465.

Chassis mounted plug P3 is mainly used to control motors and clutches. The typical functions of the P3 connectors are:

P3-1	TD clucth contactor
-2	TD clutch contactor
-3	Chassis ground
-4	Printer motor contactor
-5	Printer motor contactor
-6	From control panel off-line switch
-7	TD motor contactor
-8	TD motor contactor
-9	TD motor contactor
-10	Off-line slave relay contact
-11	
-12	Off-line slave relay contact
-13	

4. CALIBRATION AND ADJUSTMENTS

The only units within a Model 431 Selector that require calibration and adjustment are the Signal Distributor and Distortion Monitor printed circuit boards. Refer to the individual manuals for calibration proceedures.

5. THEORY OF OPERATION

5.1 General - The electronic control circuitry for the model 431 Solid State Selector is housed on plug-in printed circuit modules. A few control functions are relay controlled. The associated relays along with the input and output relays if used in place of the EIA Interface are mounted on the main chassis.

The following circuit description is divided into two parts. First, there is a functional description that presents the overall data flow and control logic by referring to the simplified block diagram. Second, there is a circuit description using the main assembly schematic diagram to show the actual circuits.

A detailed circuit description for each plug-in board is given in supplementary manuals at the rear of this manual. Notice that certain portions of the plug-in boards go unused in the Model 431 selector. This is because the boards used are universal types that have been strapped for use by this system.

5.2 Functional Description - The selector has six printed circuit boards, including the power supply and optional parity checker. Each provides a specific function. The Signal Distributor (SD) receives data from and transmits answer back characters through the EIA interface. The optional Parity Checker (PC) checks each incoming character for even parity, and substitutes a predetermined character for any data character found in error. The function (F) board examines each incoming character, looking for and responding to appropriate control characters. The distortion monitor checks incoming data for excess distortion. The EIA interface board translates operating levels from the line to the logic.

5.2.1 Signal Distributor (SD) The signal distributor receives data into its shift register (7). When the loop goes spacing during the start pulse the clock (8) will begin to run, putting out a pulse at the center of each mark or space.

These clock impulses will shift the character into the shift register one bit at a time. When the character is fully loaded, the register loaded line will cause circuit 6 to send out a pulse. This pulse is used by the Function and Parity Checker.

The signal distributor also generates and transmits the answer back signals. Circuits 1 and 4 combine to give a ready-to-receive/no-traffic answer back, and circuits 2 and 3 combine to give the unable-to-receive answer back. For example: if a no-traffic answer back is required gate C will condition gates 1 and 4. The output for gate 1 will set a S2 character into the shift register through diode matrix A, and the gate 1 output will also gate the delay network through diode matrix A, and the gate 1 output will also gate the delay network through gate K. After the S2 has been transmitted, the delay will pulse gate 4. This pulse along with the output of gate C will set the stations alpha character into the register through diode matrix B. Then the alpha character will be transmitted. An unable-to-receive (BELL or FE_o) is transmitted in a similar fashion by gates 2 and 3.

In summary, the key to the signal distributor is the shift register. It receives data from the loop in serial form. It presents data to the Parity Checker and Function circuits in parrallel form, and it sends answer backs to the loop in serial form.

5.2.2 Parity Checker (PC) - The parity checker is used to check incoming data for even parity. The PC flip-flop monitors the incoming line. Each time the signal distributor clock (8) pulses a bit into the SD shift register (7), the PC flip-flop is also pulsed. If a mark is present, the flip-flop will change state. It follows that if an even number of marks occur during any one character time the flip-flop will return to its initial state on the last mark.

When the character is completely loaded into the SD shift register, the register loaded line will become active and cause SD circuit 6 to pulse its output line. This pulse enables gates 1 and 2 in the PC. If there was no error, gate 2 will set the substitution character into the shift register (5).

When a character is set into the shift register, the clock will run until the character has been transmitted through the serial output. The PC serial output goes to the printer.

In summary, the key to the parity checker is the PC flip-flop. The flip-flop monitors the incoming character. After the character is loaded into the signal distributor, the PC flip-flop determines whether the data or the substitution character is to be loaded into the PC shift register (5) for use by the printer.

If the parity checker option is not selected, data is sent directly from the Signal Distributor to the selector magnet.

5.2.3 Function Board (F) - The function board examines each incoming character to determine whether or not it is a control character, and responds accordingly. The codes and their functions are listed in Table 4-1.

TABLE 4-1

Control characters, their mnemonic codes, characters, and functions

MNEMONIC	CHAR.(S)	FUNCTION
SOT	SOT	START OF TRANSMISSION - Releases any preselected TD to send message FDX and sets any selected printer to non-select printing mode.
EOT	EOT	END OF TRANSMISSION - Sets all printers to non-printing select mode.
INT	NULL	INTERRUPT - Place printers in non-print mode and stops any sending TD.
X-OFF	X-OFF	STOP TD - Resets any selected TD to non-select mode.

MNEMONIC	CHAR. (S)	FUNCTION
1st TSC	DC_o	FIRST TRANSMITTER START CODE - The first character of a two character series is used to select any TD.
2nd TSC	Alpha Char.	SECOND TRANSMITTER START CODE - When preceded by a 1st TSC, this character causes the tape reader to start, or the no-traffic answer back to be send.
1st RSC	S_1	FIRST RECEIVER START CODE - This first character of a two character series is used to select any printer.
2nd RSC	Alpha Char.	When preceded by a 1st RSC, this character causes the printer to be selected.

To facilitate the explanation, it will be assumed that no message is being transmitted or received, and that the transmit and receive loops are marking.

The following sequence of events will be described:

(1) Processor polls for traffic
(2) Processor sends a message
(3) During processor's message, the traffic ends
(4) Processor interrupts message and polls for additional traffic
(5) Processor resumes sending until message is complete

(1) Processor polls for traffic - In order for the processor to poll the station for traffic, it sends a TSC followed by the station's discrete alpha character. These characters will be presented to the Function's decode matrix (9). First, the 1st TSC will set the 1st flip-flop through gate 1. Next, the 2nd TSC will be gated through gate 3 to set the 2nd TSC flip-flop. Notice that gate 1 is conditioned by the SOT flip-flop. The SOT flip-flop is used to condition gates 1 and 2 during the select mode. The 2nd TSC flip-flop conditions gates 5 and 6. If the TD is ready, gate 5 will pass the run signal. If the TD is not ready, gate 6 will initiate a no-traffic answer back by going through gate 6 (refer to paragraph 5.2.1 for an explanation of answer back).

(2) Processor sends a message - The processor sends a message to one or more stations by sending the Receiver Start Code (RSC) followed by a Start-of-Transmission (SOT) character.

The RSC is a two character sequence. The first character (1st RSC) is the same for any station: it is an S_1. The second character (2nd RSC) is the station's unique alpha character. These two characters are acted on when they are received in sequence, and when the SOT flip-flop is reset to signify that the select mode is in effect.

When a station is addressed to receive a message, it will send an answer back to indicate a printer-ready or printer-not-ready condition. The station must have the send side of the full-duplex loop to do this. Therefore, each RSC sequence, addressing one or more stations, will be preceded by an interrupt character (INT). The reception of the INT character will set the INT flip-flop. When set, the INT flip-flop inhibits the TD by disabling gate 5, and the printer by disabling gate 7. With the INT flip-flop set, the station can receive control codes and respond with answer backs without printing the control characters and without inteferring with the message from the TD.

The 1st RSC will pass through gate 2 and set the 1st RSC flip-f'op. Setting the 1st RSC flip-flop conditions gate 4. The 2nd RSC character will now pass through gate 4 and set the 2nd RSC flip-flop. When the 2nd RSC flip-flop changes is set, it causes circuit 8 to send a pulse over its output line. The pulse from circuit 8 conditions circuits b and c. If the printer is ready, circuit b will pass the pulse and cause a ready-to-receive answer back to be generated by the signal distributor. If the printer is not ready, due to low paper, a bell answer back is given. Circuit c will initiate a bell if the station is not ready, due to being off line, a FE_o answer back is given.

When the processor has addressed all desired stations and received their answer back, a SOT (start-of-transmission) character will be sent. This character sets the SOT flip-flop to prevent selection during the message text. The SOT also resets the INT flip-flop to release the printer (via circuit 7) and the TD (via circuit 5).

(3) With a TD sending to the processor, and with the processor sending to a printer, the message on the TD ends. The EOT on the tape will be recognized by the processor and cause the processor to send a INT character. This INT character will stop the TD and printer. Then an X-OFF character will disconnect the TD. Following this INT X-OFF sequence, the processor will again poll for traffic from a TD, and when the polling ends, re-start the printer.

5.2.4 Distortion Monitor - The Distortion Monitor checks incoming signals for distortion in excess of 25 or 37 1/2% (strap selectable). When the station is in the receive mode, data will pass through distortion monitor gate 1 to the distortion check circuit. Excess distortion will cause the control panel mounted distortion lamp to flash.

5.3 Main Chassis Description - The main chassis holds the wiring and sockets needed to connect the relays and printer circuit modules. A functional description is given in paragraph 5.2. This paragraph is keyed to the functional description, and will list each major component's function so that it may be associated with the functional description. Descriptions of circuitry within the printed circuit modules can be found in individual PC board manuals at the rear of this manual.

5.3.1 Signal Distributor J1 - The signal distributor (SD) receives data from the loop in serial form and stores it in the shift register. Data is fed into the SD through pin H. Data is taken from the SD in both serial and parallel form. Parallel data is on pins 21, 14, 15, 22, 16, 17, 18 and 19 for bits 8 through 1 respectively. This parallel data is set into the Function and Parity Checker boards by an inpulse that appears on pin 20. The Function board also uses the timing pulse at pin 9. This pulse occurs at the center of the pulse on pin 20.

The answer backs are controlled by input pins J, L, 11 and 13. To send a ready-to-receive or no-traffic answer back, pins 13 and J go open or high. To send a low-forms or off-line answer back, pins L and 11 go open or high. The answer backs are driven out pin Z to the output circuits.

The SD clock running signal is fed to the Parity Checker through pin 6. Pin 7 supplies the Parity Checker with the 50% flip-flop clock signal from the signal distributor.

5.3.2 Parity Checker J3 - The Parity Checker receives data in parallel form from the signal distributor. Pins W. V, U, T, Z, S. R, and Y receive bits 1 through 8, respectively. Pin X receives the gate pulse when the character is complete. Pin H receives the 50% flip-flop from the signal distributor to clock the parity check flip-flop. Pin F receives the SD clock running signal.

5.3.3 Eight Level Function J5 - The function board responds to control characters. Pins W, V, U, T, Z, S, R and Y receive bits 1 through 8, respectively. Pin X receives the data gate. Pin K receives the reset pulse. Pins 1 and 4 put out a pulse when the 2nd RSC flip-flop is set. If the forms-low or off-line relay is up, the pulse at pin 1 will be returned to pin 6 to reset the 2nd RSC flip-flop, and the pulse at pin 4 will cause the signal distributor to send a bell or FE_o answer back.

Pin 7 will go low when there is no tape in the gate. Pin 8 going low will cause the signal distributor to send a no-traffic answer back. Pin 5 goes low during the select printing mode to enable the parity checker.

Pin E will go high as a result of the open relay operating. When pin E goes high, pin 2 will go low to energize the Xmit alarm relay.

Pin 3 will go low to energize the printer motor controller relay, S2, when the non-select print mode is in effect. Pin D will go low to energize TD clutch control relay, S1, when in the transmit mode.

Pin M will go low to reset the 2nd TSC flip-flop, should tape run out of the transmitter (tape out).

5.3.4 Relays - Several functions are relay controlled. The following paragraphs describe each relay's function.

TAPE RELAY K1 - The tape relay is energized when tape is in the gate, ready to send.

XMIT ALARM K2 - This relay will be energized when the receive loop opens during a tape transmission. To be reset, the tape gate must be opened and the external reset pushbutton must be depressed - in that order.

LOW FORM K3 - When the printer's paper supply is low, this relay will be energized.

OFF LINE K4 - Switching to off line will energize K4.

OFF LINE SLAVE S4 - Operating with K4.

CLUTCH K5 - The TD clutch will be energized during transmission when K5 is energized.
PRINTER MOTOR S3 - During receive, relay S2 will be energized to run the printer motor.
PRINTER MOTOR S2 - The transmitter-distributor motor is energized through S3 contacts during the transmission of a tape.

TD ON/OFF LINE S1 - Operates when TD switched off line.

5.4 Strapping Options - The strapping options on the printed circuit boards are detailed in each board's individual manual included at the rear of this manual.

6. ORDERING INFORMATION

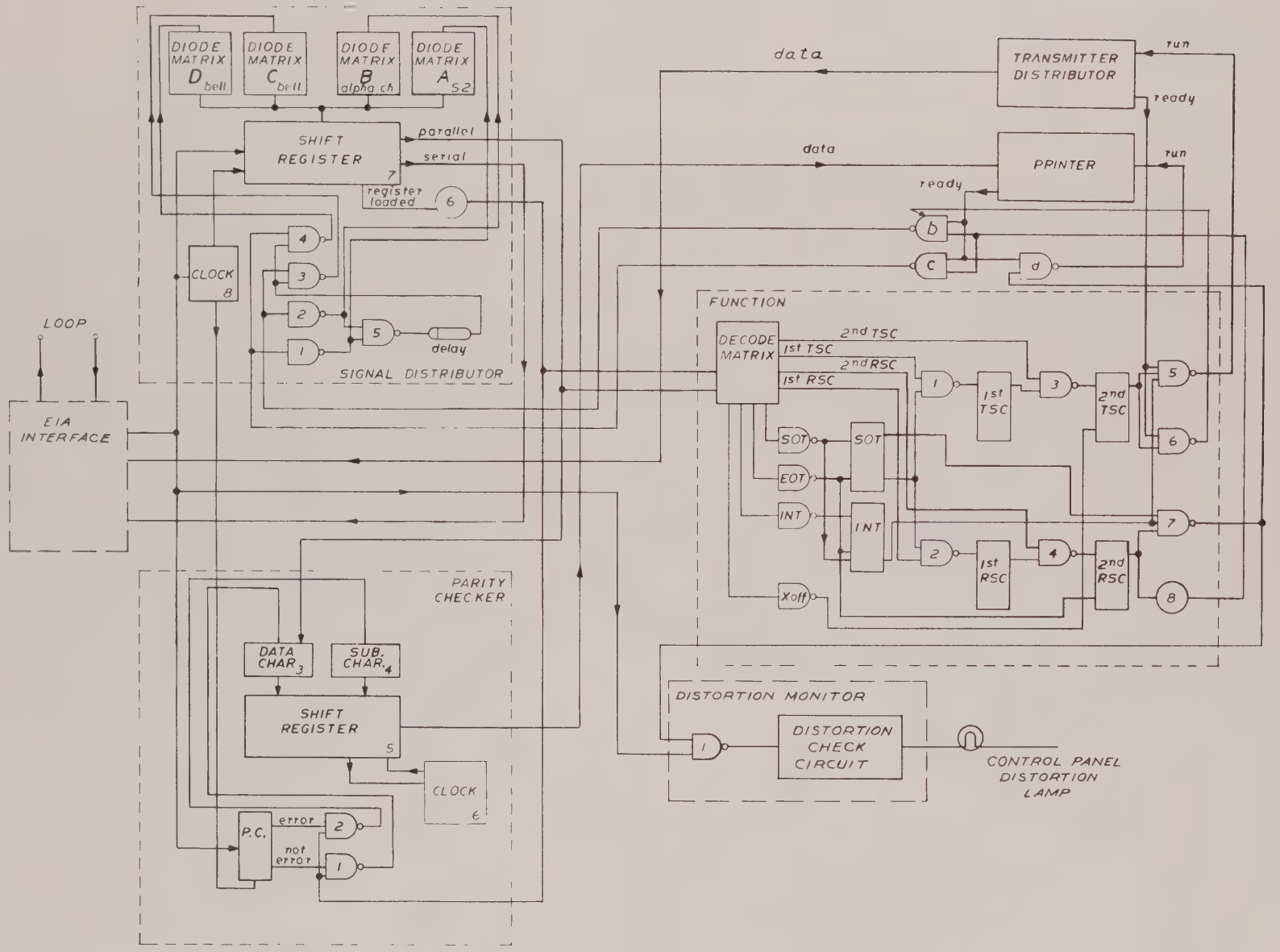
Order From

Pulse Communications, Inc.
5714 Columbia Pike
Falls Church, Virginia 22041

Telephone - (703) 820-0652
Telex - 89-9423

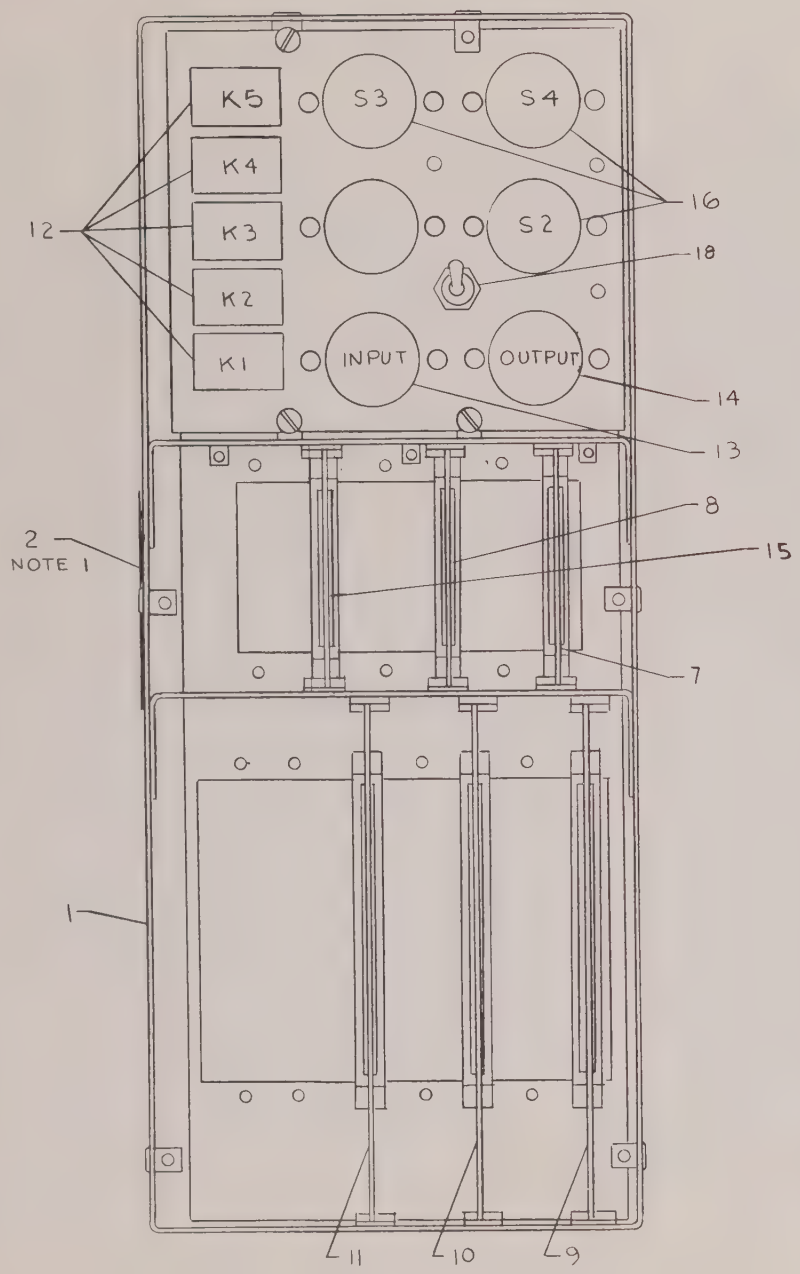
7. DRAWINGS

C100453	Assembly, Model 431 Selector
D200465	Schematic, Model 431 Selector
C100455	Assembly and Schematic, Model 6006-2 Control Panel
E200407	Schematic, 8-Level Function No. 2 showing programming straps for Half-Duplex operation (HDX) in a Model 431
E200407	Schematic, 8-Level Function No. 2 showing programming straps for Full-Duplex operation (FDX) in a Model 431
E200363	Schematic, Multi-Level Signal Distributor showing programming straps in a Model 431



431-10 Functional Block Diagram.

REVISIONS					
NO/SYM	DESCRIPTION	DATE	BY	CHK	APPD



NOTES:

1. INFORMATION TO BE TYPED IN "431-10" & SERIAL NO.

QTY REQD -1	CODE IDENT NUMBER	PART OR IDENT NUMBER	ITEM	NOMENCLATURE OR DESCRIPTION	NOTES & REF DESIGNATIONS
			19		
1		3490-0018	18	SWITCH, TOGGLE	SW1
1		B500621	17	EXTRACTOR, P.C. BD	
3		3664-0009	16	RELAY	S2, S3, S4
1		C100452-1	15	PC BOARD ASSY	
REF		3468-0008	14	RELAY	OUTPUT
REF		3468-0010	13	RELAY	INPUT
5		3664-0012	12	RELAY	K1 THRU K5
1		D100408-1	11	PC BOARD ASSY	
1		D100321-1	10	PC BOARD ASSY	
1		D501377-2	9	PC BOARD ASSY	
1		C100432-1	8	PC BOARD ASSY	
1		C500711-2	7	PC BOARD ASSY	
REF		D200465	6	SCHEMATIC	
1		3649-0004	5	CONNECTOR RECEPT	
2		3649-0003	4	CONNECTOR PLUG	
3		3649-0005	3	STRAIN RELIEF	
1		B500802	2	PLATE IDENT	
1		D500896-12	1	SELECTOR SUBASSY	

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TOLERANCES:

2 PLACE DECIMALS ± —

3 PLACE DECIMALS ± —

ANGLES ± —

DO NOT SCALE DRAWING

MATERIAL:

FINISH:

DRAWN W. GLEADALL 16 SEPT 69 DATE

CHECKED DATE 3/25/70

PROJ ENGRG DATE 3/25/70

PROD ENGRG DATE 3/25/70

M H Jones QC 23 Mar 70

CAUTION: UNLESS THIS DRAWING BEARS THE NAMES OF THE "PROJ ENGRG." "PROD ENGRG." IT IS PRELIMINARY AND UNDER NO CIRCUMSTANCES IS IT TO BE USED FOR MANUFACTURING PURPOSES

THIS DRAWING IS FURNISHED FOR ENGINEERING INFORMATION AND REFERENCE ONLY. THE FURNISHING OF THIS DRAWING DOES NOT CONVEY ANY REPRODUCTION OR MANUFACTURING RIGHTS.

PULSECOM

PULSE COMMUNICATIONS, INC.
ALEXANDRIA, VA.

SELECTOR ASSEMBLY (MODEL 431-10)

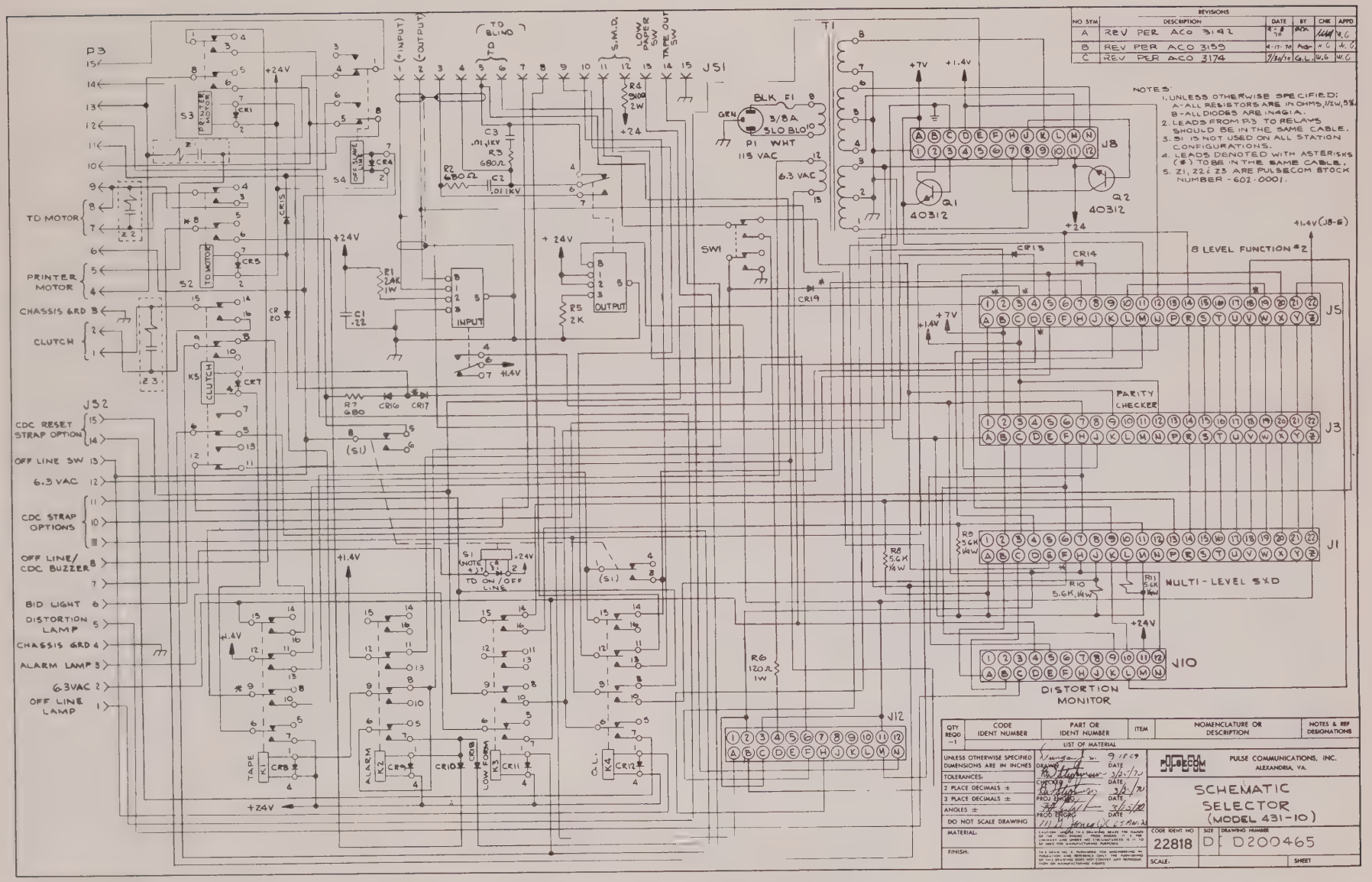
CODE IDENT NO. 22818

SIZE C

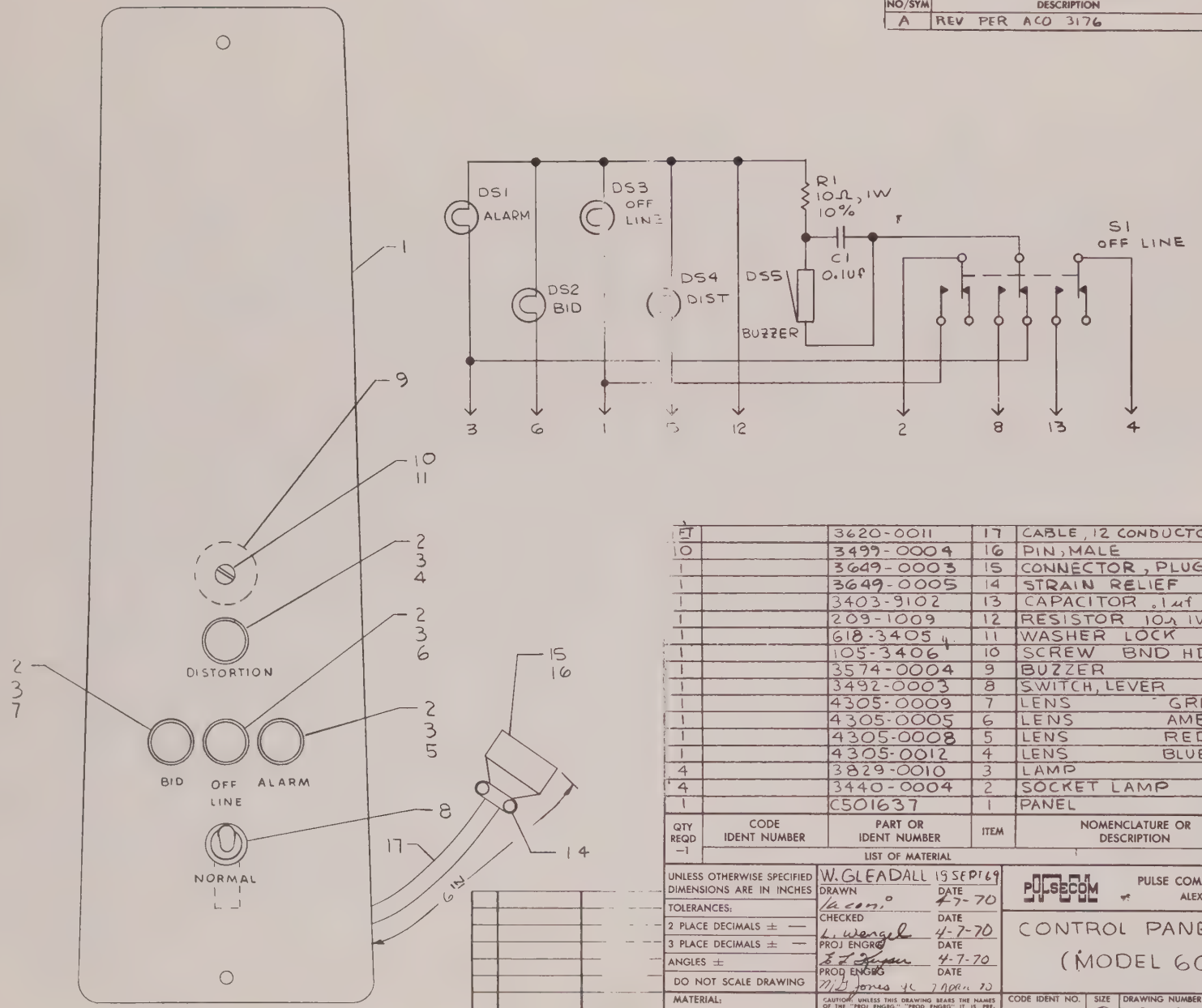
DRAWING NUMBER C100453

SCALE: 1/1

SHEET


REVISIONS
NO SYM | DESCRIPTION | DATE | BY | CHK | APPD
A | REV PER ACO 3192 | 4-8-70 | BRSK | WWH | W.G
B | REV PER ACO 3159 | 4-17-70 | RGP | W.G | W.G
C | REV PER ACO 3174 | 7/30/70 | G.L. | W.G | W.G
NOTES:
1. UNLESS OTHERWISE SPECIFIED:
A-ALL RESISTORS ARE IN OHMS, 1/2W, 5%
B-ALL DIODES ARE IN4934.
2. LEADS FROM P3 TO RELAYS SHOULD BE IN THE SAME CABLE.
3. S1 IS NOT USED ON ALL STATION CONFIGURATIONS.
4. LEADS DENOTED WITH ASTERISKS (*) TO BE IN THE SAME CABLE.
5. Z1, Z2 & Z3 ARE PULSECOM STOCK NUMBER - 602-0001.
P3
J51
T1
J8
Q1 40312
Q2 40312
J5
8 LEVEL FUNCTION #2
J3
PARITY CHECKER
J1
MULTI-LEVEL SXD
J10
DISTORTION MONITOR
J12
J52
TD MOTOR
PRINTER MOTOR
CHASSIS GRD 3
CLUTCH
CDC RESET STRAP OPTION
OFF LINE SW 13
6.3 VAC
CDC STRAP OPTIONS
OFF LINE/ CDC BUZZER
BID LIGHT 6
DISTORTION LAMP 5
CHASSIS GRD 4
ALARM LAMP 3
6.3VAC 2
OFF LINE LAMP 1
TAPE
ALARM
LOW FORM
C.L.
INPUT
OUTPUT
TD ON/OFF LINE
TD BLIND
S.M.D.
LOW PAPER SW
TAPE OUT SW
BLK F1
GRN
WHT
115 VAC
6.3 VAC
+24V
+7V
+1.4V
+1.4V(J8-E)
QTY REQD | CODE IDENT NUMBER | PART OR IDENT NUMBER | ITEM | NOMENCLATURE OR DESCRIPTION | NOTES & REF DESIGNATIONS
LIST OF MATERIAL
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES:
2 PLACE DECIMALS ±
3 PLACE DECIMALS ±
ANGLES ±
DO NOT SCALE DRAWING
MATERIAL
FINISH
DRAWN 9/16/69
CHECKED 3/5/70
PROJ ENGR 3/5/70
PROD ENGR
PULSECOM
PULSE COMMUNICATIONS, INC.
ALEXANDRIA, VA.
SCHEMATIC
SELECTOR
(MODEL 431-10)
CODE IDENT NO 22818
SIZE D
DRAWING NUMBER D200465
SCALE
SHEET

REVISIONS					
NO/SYM	DESCRIPTION	DATE	BY	CHK	APPD
A	REV PER ACO 3176	5/1/70	W.G.	WM	W.C.



QTY REQD -1	CODE IDENT NUMBER	PART OR IDENT NUMBER	ITEM	NOMENCLATURE OR DESCRIPTION	NOTES & REF DESIGNATIONS
FT		3620-0011	17	CABLE, 12 CONDUCTOR	#22
10		3499-0004	16	PIN, MALE	
1		3649-0003	15	CONNECTOR, PLUG	
1		3649-0005	14	STRAIN RELIEF	
1		3403-9102	13	CAPACITOR .1uf	C1
1		209-1009	12	RESISTOR 10Ω 1W 10%	R1
1		618-3405 4	11	WASHER LOCK	#6
1		105-3406	10	SCREW BND HD	6-32 x 7/16
1		3574-0004	9	BUZZER	DS5
1		3492-0003	8	SWITCH, LEVER	S1
1		4305-0009	7	LENS GRN	
1		4305-0005	6	LENS AMB	
1		4305-0008	5	LENS RED	
1		4305-0012	4	LENS BLUE	
4		3829-0010	3	LAMP	DS1 THRU DS4
4		3440-0004	2	SOCKET LAMP	
1		C501637	1	PANEL	

LIST OF MATERIAL

DASH NO	NEXT ASSY	USED ON
1		

APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES:
2 PLACE DECIMALS ± —
3 PLACE DECIMALS ± —
ANGLES ±
DO NOT SCALE DRAWING
MATERIAL: —
FINISH: —

DRAWN	W. GLEADALL 19 SEPT 69	DATE 4-7-70
CHECKED	L. Wengel	DATE 4-7-70
PROJ ENGR'G	E. L. Hyman	DATE 4-7-70
PROD ENGR'G	W. B. Jones 4C	DATE 7 APR 70

CAUTION: UNLESS THIS DRAWING BEARS THE NAMES OF THE "PROJ ENGR'G." "PROD ENGR'G" IT IS PRELIMINARY AND UNDER NO CIRCUMSTANCES IS IT TO BE USED FOR MANUFACTURING PURPOSES

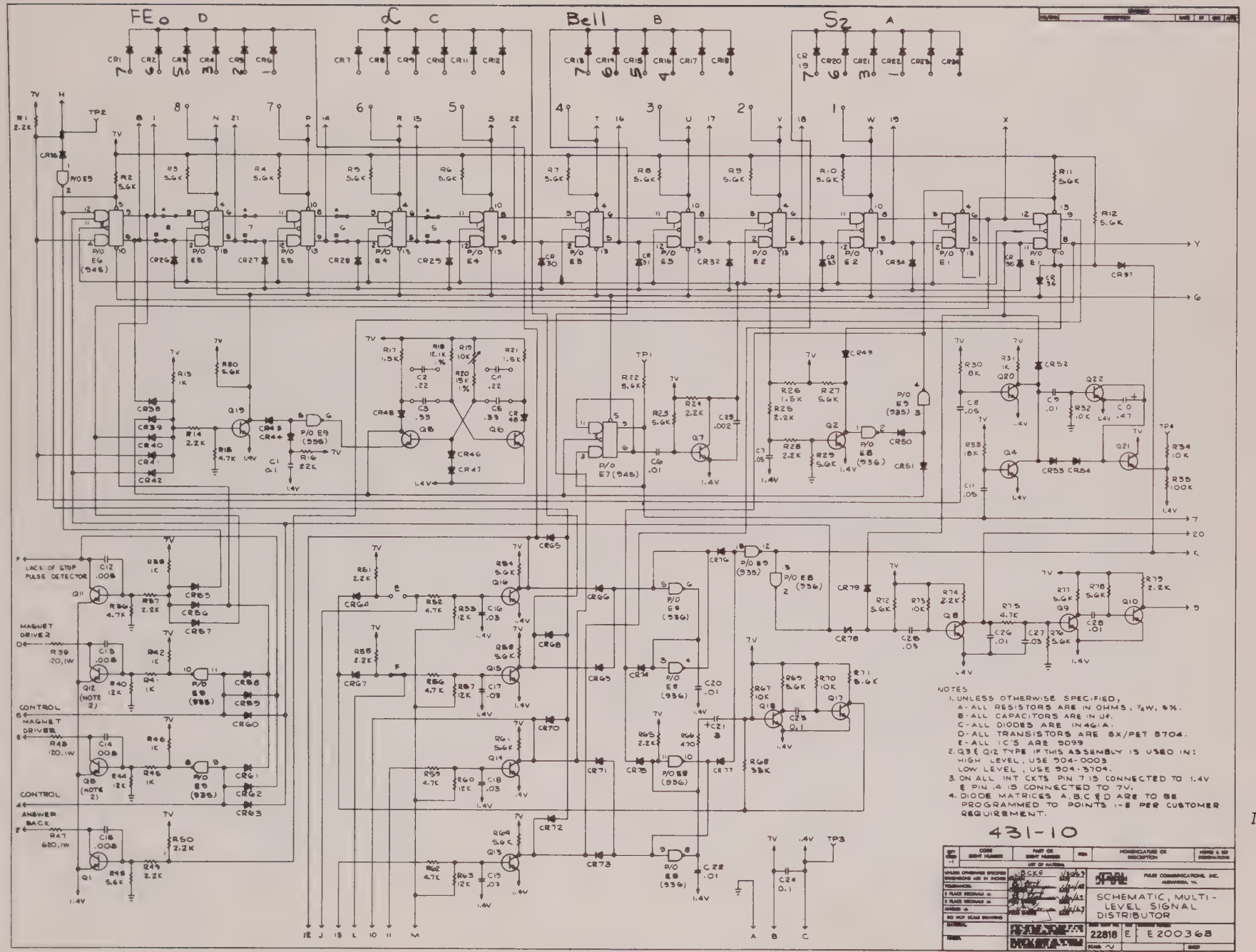
THIS DRAWING IS FURNISHED FOR ENGINEERING INFORMATION AND REFERENCE ONLY. THE FURNISHING OF THIS DRAWING DOES NOT CONVEY ANY REPRODUCTION OR MANUFACTURING RIGHTS

PULSECOM — PULSE COMMUNICATIONS, INC. ALEXANDRIA, VA.

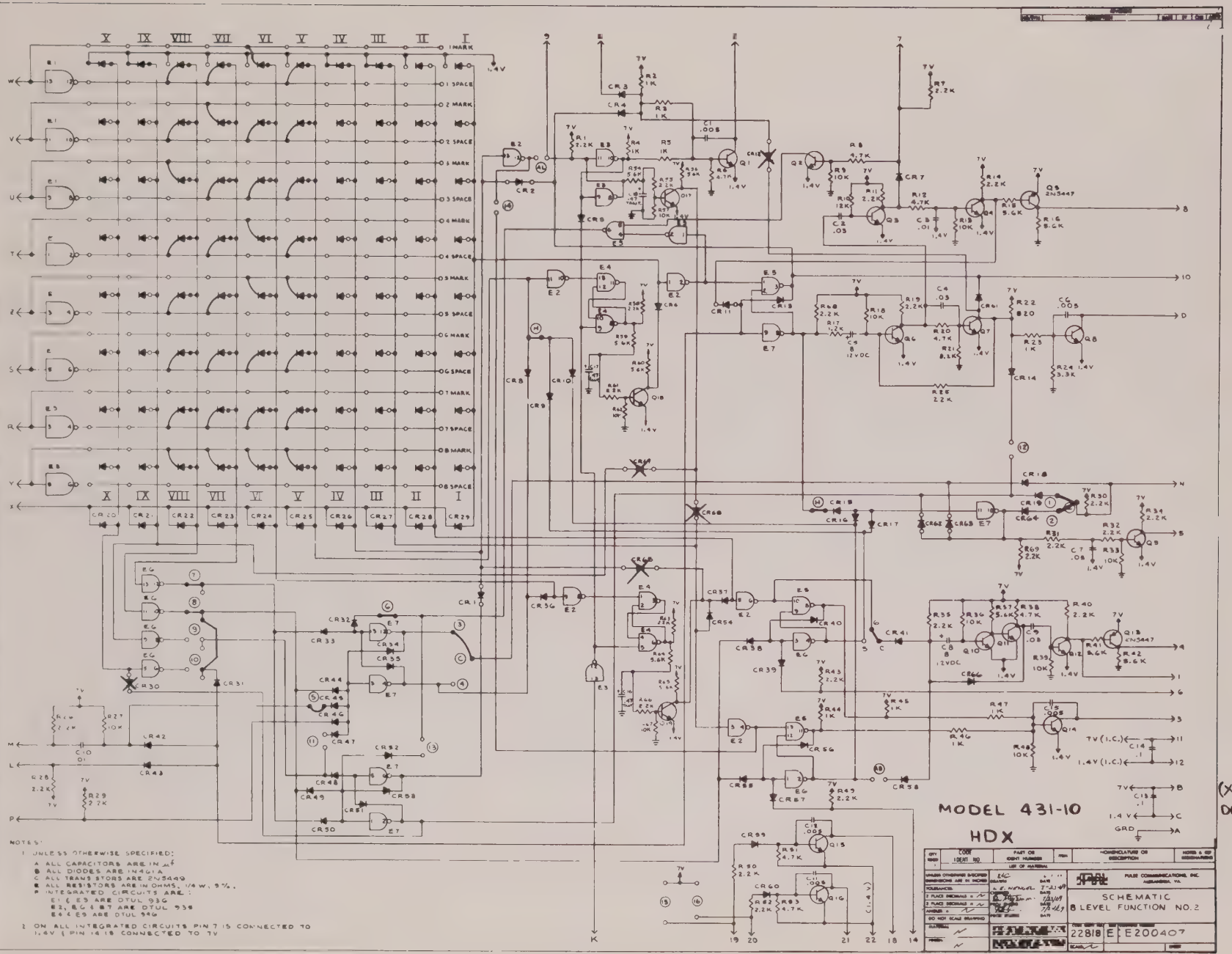
CONTROL PANEL ASSY (MODEL 6006-2)

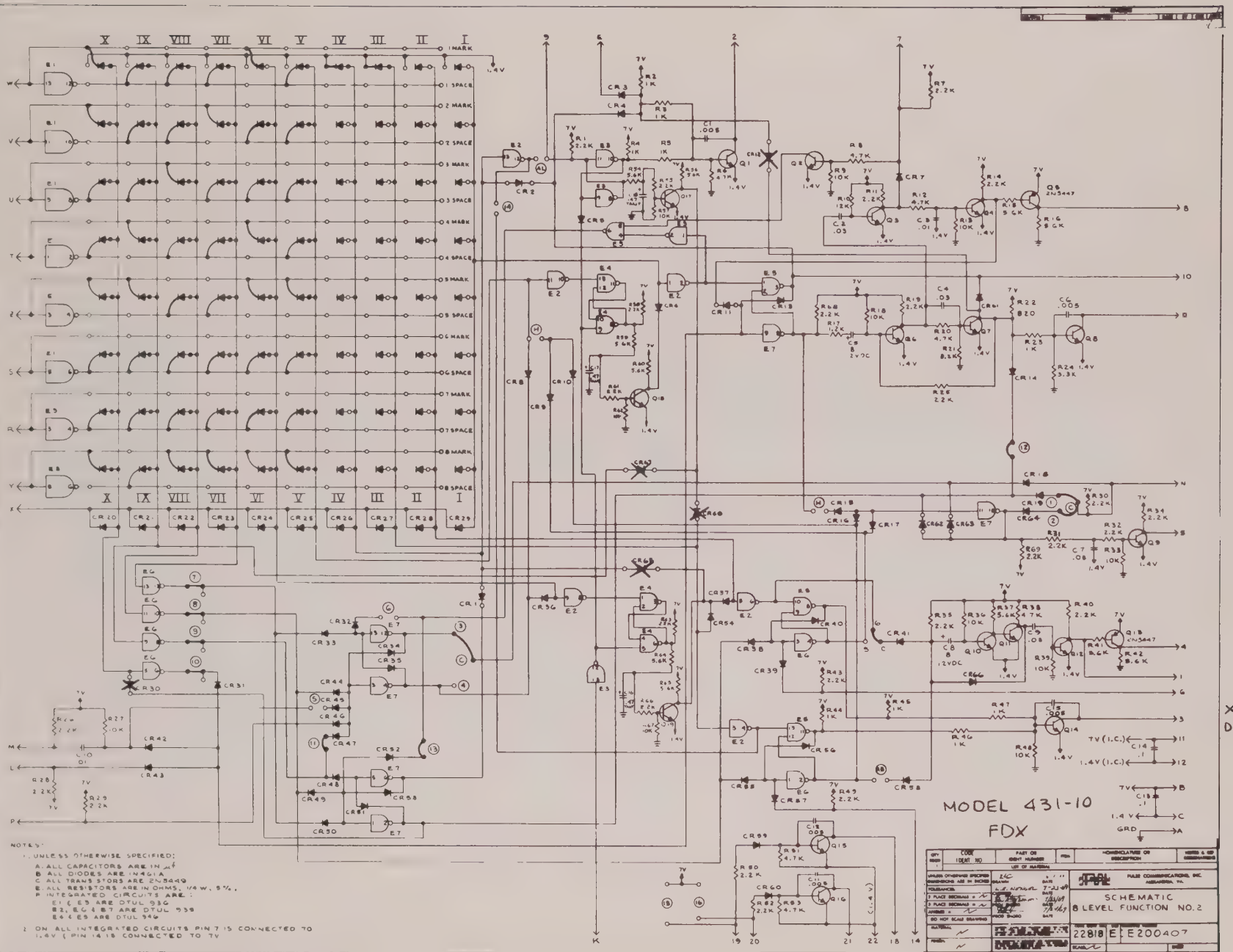
CODE IDENT NO.	SIZE	DRAWING NUMBER
22818	C	C100455

SCALE: 1/1 SHEET


FE o D
C C
Bell B
S2 A
NOTES
1. UNLESS OTHERWISE SPECIFIED,
A - ALL RESISTORS ARE IN OHMS, ¼W, 5%.
B - ALL CAPACITORS ARE IN Uf.
C - ALL DIODES ARE IN4614A.
D - ALL TRANSISTORS ARE 6X/PET 5704.
E - ALL IC'S ARE 9099
2. Q3 & Q12 TYPE IF THIS ASSEMBLY IS USED IN:
HIGH LEVEL, USE 904-0003
LOW LEVEL, USE 904-3704.
3. ON ALL INT CKTS PIN 7 IS CONNECTED TO 1.4V
& PIN 14 IS CONNECTED TO 7V.
4. DIODE MATRICES A, B, C & D ARE TO BE PROGRAMMED TO POINTS 1-8 PER CUSTOMER REQUIREMENT.
431-10
SCHEMATIC, MULTI-LEVEL SIGNAL DISTRIBUTOR
PAIGE COMMUNICATIONS, INC.
ALEXANDRIA, VA.
22818
E
E 200368

I-2


MODEL 431-10
HDX
SCHEMATIC
8 LEVEL FUNCTION NO.2
DATA PULSE COMMUNICATIONS, INC.
22818 E E200407
(X) = DELETE
NOTES:
1. UNLESS OTHERWISE SPECIFIED:
A. ALL CAPACITORS ARE IN μF
B. ALL DIODES ARE IN4614
C. ALL TRANSISTORS ARE 2N3449
D. ALL RESISTORS ARE IN OHMS, 1/4 W, 5%.
E. INTEGRATED CIRCUITS ARE:
E1 & E5 ARE DTUL 936
E2, E6 & E7 ARE DTUL 934
E3 & E4 ARE DTUL 946
2. ON ALL INTEGRATED CIRCUITS PIN 7 IS CONNECTED TO 1.4V & PIN 14 IS CONNECTED TO 7V


MODEL 431-10
FDX
SCHEMATIC
8 LEVEL FUNCTION NO.2
22818 E 200407
X = DELETE
NOTES:
1. UNLESS OTHERWISE SPECIFIED:
A. ALL CAPACITORS ARE IN μf
B. ALL DIODES ARE IN4614
C. ALL TRANSISTORS ARE 2N3449
D. ALL RESISTORS ARE IN OHMS, 1/4 W, 5%.
E. INTEGRATED CIRCUITS ARE:
E1 (E3 ARE DTUL 936
E2, E6 & E7 ARE DTUL 939
E4 & E5 ARE DTUL 946
2. ON ALL INTEGRATED CIRCUITS PIN 7 IS CONNECTED TO 1.4V (PIN 14 IS CONNECTED TO 7V

INSTRUCTION MANUAL

8-LEVEL FUNCTION #2
Model D100408

Issue 2
IN#183
(3/70)

Pulse Communications, Inc.
5714 Columbia Pike
Falls Church, Virginia 22041
Telephone: (703) 481-0652
Telex: 89-9423

IN#183
(3/70)

8-LEVEL FUNCTION #2

Model D100408

Issue 2

TABLE OF CONTENTS

	Page
1. GENERAL	1
2. SPECIFICATIONS	1
3. INSTALLATION	2
4. THEORY OF OPERATION	7
5. ORDERING INFORMATION	20
6. DRAWINGS	20

8-LEVEL FUNCTION #2

Model D100408
Issue 2

1. GENERAL

The Model D100408 8-Level Function #2 printed circuit board is used in PULSECOM Solid State Selectors to detect and respond to control characters. This board is able to detect 10 characters through a programmable diode matrix. Each of the 10 characters may consist of any combination of marks and spaces. Thus, any 8-level code can be accommodated, such as that used in the 8B1 scheme. Input in parallel form is accepted from the Signal Distributor printed circuit board in the Selector.

After a control character or sequence has been recognized, output lines will activate relays and circuits to control the telegraph station. In addition to station control, the 8-Level Function #2 board initiates the answerback signals.

The condition of the station, such as low paper, is continuously monitored. If a TSC or RSC is received, this board will initiate a ready-to-receive or not-ready answerback, depending on the station's status.

Half- or full-duplex operation is provided by strapping options.

2. SPECIFICATIONS

Voltage Requirements	+7 v dc, +1.4 v dc (used as a reference) these operating voltages are supplied by the selector.
External Connections	Plug into sockets in selector
Logic Levels:	
a. Binary 1 (High)	+5 volts nominal (greater than +2.5 volts above reference)
b. Binary 0 (Low)	0 volts nominal (less than +1.0 volt above reference)

Code Sequences:

(NOTE: Any function listed may be omitted at customer's option.)

a. Receiver Start Code (RSC): Two, two character sequences. Sequences are diode programmed. One for the station, second for broadcast (first character common to both). RSC activates printer motor and initiates answerback. In broadcast mode, one outstation is programmed for answerback (usually last station of polling sequence).

b. Start of Text (STX): Single, diode programmable character. Enables selector magnet. Inhibits further selection (RSC or TSC). Enables interrupt (INT) detection circuits.

c. End of Text (ETX): Single character, diode programmable. Terminates transmitter-distributor operation. Reestablishes TSC sequence.

d. End of Transmission (EOT): Single character, diode programmable. Terminates printer operation by inhibiting the selector magnet. Reestablishes RSC and interrupt detection circuits.

e. Interrupt (INT): Single character, diode programmable. Strap selectable. Inhibits operating printers and transmitter-distributors to allow polling.

f. Transmit Start Code (TSC): Two characters, diode programmed. If no tape is in gate, a "no traffic" answerback is initiated.

g. Emergency Stop: Two characters, diode programmed. INT and character IV (emergency stop). Note that the character IV does not have to directly follow interrupt. This space allows the interjection of a service message before the station is locked out. Stops TD, if sending, and stops printer, if receiving.

3. INSTALLATION

The 8-Level Function #2 P.C. board mounts in a 44 pin (22 pin, double sided) P.C. edge connector, Cinch Mgf. Co. #251-22-30-160 or equivalent. Refer to Table 3-1 for pin number assignment and function.

3.1 Programming

There are two groups of straps that must be connected to allow the 8-Level Function #2 board to be used in a particular system. The system manual will have a schematic diagram showing the connections for that particular system.

Table 3-2 lists the straps and their usual function. To determine exactly how the board is strapped for an individual system, refer to the system manual.

The decode matrix is programmed to respond to certain characters. The 10 available characters are programmed by installing diodes in the matrix. There will be one diode for each mark or space of each character. For example: If Row X is to be an 8-level control C (ETX), the diodes will be set to detect MMSSSSSS as shown in Figure 4-3. If a character is not to be used, the bit 1 diodes is connected to the 1.4 volt buss (reference) to delete that position.

Table 3-1
Pin Number/Function

Pin No.	Function
1	Q12 output (NH): used to provide 150 microsecond pulse (NH-L-H) for resetting the Broadcast RSC detection flip-flop for circuit testing.
2.	Q1 output (NH): used to drive Xmit Alarm Relay or similar device.
3	Q14 output (NH): used to drive relay for applying power to printer motor on RSC detection.
4	Q13 output (NL): used to pulse answerback circuit on Signal Distributor on RSC detection.
5	Q9 output (NH): complement of selector magnet control gate signal.
6	Reset lead from Low Form relay for resetting station RSC detection flip-flop.
7	Inhibit line from Tape Reader for inhibiting TSC answerback drive circuit when tape is placed in the gate.
8	Q5 output (NL): used to pulse answerback circuit on Signal Distributor on TSC detection.
9	Access lead, for external setting of Xmit Alarm flip-flop.
10	TSC detection flip-flop output at E5-3: used to drive external indication of TSC reception.
11	+7 volts (for integrated circuits)
12	+1.4 volts (for integrated circuits)
13	Open pin
14	Reset lead for resetting Broadcast RSC detection flip-flop
15	Open pin
16	Open pin
17	Open pin
18	Q15 output; auxiliary inverter

Table 3-1
Pin Number/Function (continued)

Pin No.	Function
19	Input lead for controlling auxiliary inverter Q15
20	Input lead for controlling auxiliary inverter Q16
21	Q15 output; auxiliary inverter
22	1.4 volts (reference voltage for Q15 and Q16)
A	Ground
B	+7 volts
C	+1.4 volts
D	Q8 output (NH): used to drive relay for controlling TD
E	Control lead for enabling Q1, Xmit Alarm Relay driver, normally connected to Lack of Stop Pulse Alarm Relay.
F	Open pin
H	Open pin
J	Open pin
K	Read pulse input
L	TSC reset line from tape
M	TSC reset line from Tape Out Relay
N	Selector Magnet gate control lead
P	Auxiliary external reset lead for STX flip-flop
R	Bit 7 input to Decode Matrix
S	Bit 6 input to Decode Matrix
T	Bit 4 input to Decode Matrix

Table 3-1
Pin Number/Function (continued)

Pin No.	Function
U	Bit 3 input to Decode Matrix
V	Bit 2 input to Decode Matrix
W	Bit 1 input to Decode Matrix
X	Decode Matrix enable lead
Y	Bit 8 input to Decode Matrix
Z	Bit 5 input to Decode Matrix

NOTE: Open pins are sometimes used as tie points or may be bussed through.

Table 3-2

Programming Straps

Strap	Function
1	Blinds receiver on decode IX
2	Unblinds receiver on RSC
3	Inhibits receiver until STX
4	Inverted strap 3 function
5	Sets select mode
6	Enables receiver during transmission, 1/2 duplex only
7	STX gate
8	EOT gate
9	INT gate
10	ETX gate
11	Sets select mode
12	Inhibits transmission during interrupt
13	Resets interrupt on reception of TSC
14	Enables receiver for service message between alarm and EOT
15	Auxiliary driver bias
16	Auxiliary driver bias
17	Controls print enable circuitry
18	Gates optional control flip-flop
19	Clock pulse interrupt
AL	Alarm set
AB	Gates answerback to broadcast
H (two places)	Strapped for half-duplex. (1) Enables receiver on TSC. (2) Disables TSC in receive mode.

4. THEORY OF OPERATION

The theory of operation and circuit description is divided into three parts. First, a functional description is given referring to the functional block diagram (Figure 4-1). Second, general descriptions referring to simplified circuit diagrams. Third a circuit description referring to diagrams of specific circuits and the schematic diagram of the 8-Level Function #2 P.C. board, Drawing E200407.

4.1 Functional Description

The 8-Level #2 Function Board examines each incoming character to determine whether or not it is a control character, and responds accordingly. To facilitate the explanation, it will be assumed that no message is being transmitted or received, and that the transmit and receive loops are marking. The following sequence of events will be described:

(1) Processor polls for traffic (from outstation)
(2) Processor sends a message
(3) During processor's message, the outstation traffic ends, processor interrupts message and polls for additional traffic
(4) Processor resumes sending until message is complete

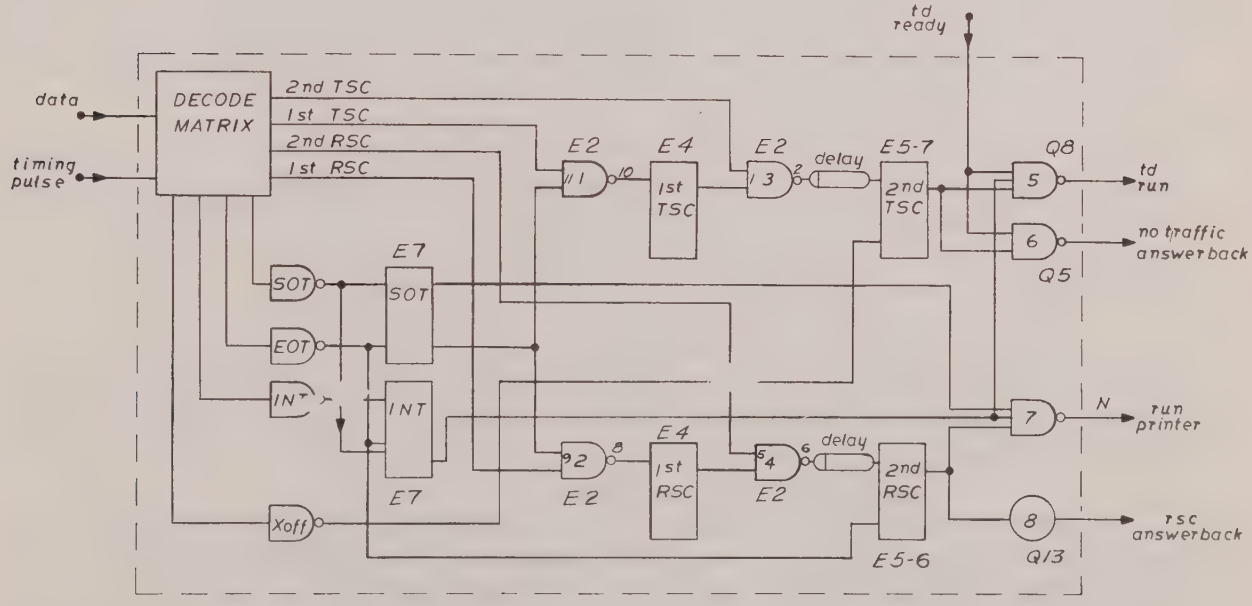


Figure 4-1. Functional Diagram

(1) Processor polls for traffic — In order for the processor to poll the station for traffic, it sends a TSC followed by the station's discrete alpha character. These characters will be presented to the function's decode matrix. First, the 1st TSC will set the 1st TSC flip-flop through gate 1. Next, the 2nd TSC will be gated through gate 3 to set the 2nd TSC flip-flop. Notice that gate 1 is conditioned by the SOH flip-flop. The SOH flip-flop is used to condition gates 1 and 2 during the select mode. The 2nd flip-flop conditions gates 5 and 6. If the TD is ready, gate 5 will pass the run signal. If the TD is not ready, gate 6 will initiate a no-traffic answerback.

(2) Processor sends a message — The processor sends a message to one or more stations by sending the Receiver Start Code (RSC) followed by a Start-of-Header (SOH) character.

The RSC is a two-character sequence. The first character (1st RSC) is the same for any station. The second character (2nd RSC) is the station's unique alpha character. These two characters are acted on when they are received in sequence, and when the SOH flip-flop is reset to signify that the select mode is in effect.

When a station is addressed to receive a message, it will send an answerback to indicate a printer-ready or printer-not-ready condition. The station must have the send side of the full-duplex loop to do this. Therefore, each RSC sequence, addressing one or more stations, will be preceded by an interrupt character (INT). The reception of the INT character will set the INT flip-flop. When set, the INT flip-flop inhibits the TD by disabling gate 5, and the printer by disabling gate 7. With the INT flip-flop set, the station can receive control codes and respond with answerbacks without printing the control characters and without interferring with the message from the TD.

The 1st RSC will pass through gate 2 and set the 1st RSC flip-flop. Setting the 1st RSC flip-flop conditions gate 4. The 2nd RSC character will now pass through gate 4 and set the 2nd RSC flip-flop. When the 2nd RSC flip-flop changes to set, it causes circuit 8 to send a pulse over its output line. The pulse from circuit 8 will initiate an answerback if the printer is ready, causing a ready-to-receive answerback to be generated.

When the processor has addressed all desired stations and received their answerback, a SOH (Start-of-Header) character will be sent. This character sets the SOH flip-flop to prevent selection during the message text. The SOH also resets the INT flip-flop to release the printer (via circuit 7) and the TD (via circuit 5).

(3) During processor's message, the outstation traffic ends. The TD will send an ETX (end of text) character to the processor. The processor will now stop and poll the stations for further traffic. First, an INT will suspend TD and printer operation at all stations. Second, an ETX character will be sent by the processor to reset the 2nd TSC flip-flop which terminates TD operation. Third, the processor will poll with TSC codes to find a message. After a message is found or if no message is found, a SOH will be sent to reset the INT flip-flop (releasing selected TD and/or printer). The SOH also sets the SOH flip-flop to establish the nonselect mode.

(4) The processor resumes sending until message is complete — When the processor has finished sending its message, it will send an EOT (end-of-transmission) character. This character

resets the SOT flip-flop to allow further selection, resets the INT flip-flop and resets the 2nd RSC flip-flop to blind the printer.

The processor is now free to send an INT and RSC's to begin the addressing for the next message.

4.2 Circuit Description

4.2.1 General. The D100408 8-Level Function #2 Board consists of three main sections. See Figure 4-2. They are as follows:

(1) Decode Matrix
(2) Detector Circuits
(3) Drive Circuits

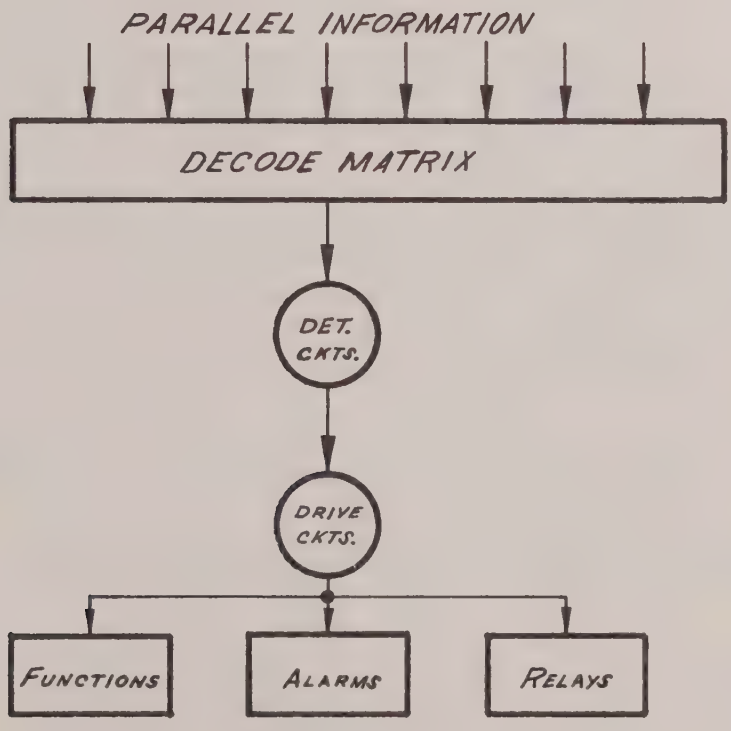


Figure 4-2. Block Diagram of 8-Level Function #2

4.2.2 Decode Matrix. An 8 x 10 matrix is used to program the marks and spaces of each character (up to ten) that is to be recognized. The following is an example of programming for ETX. See Figure 4-3.

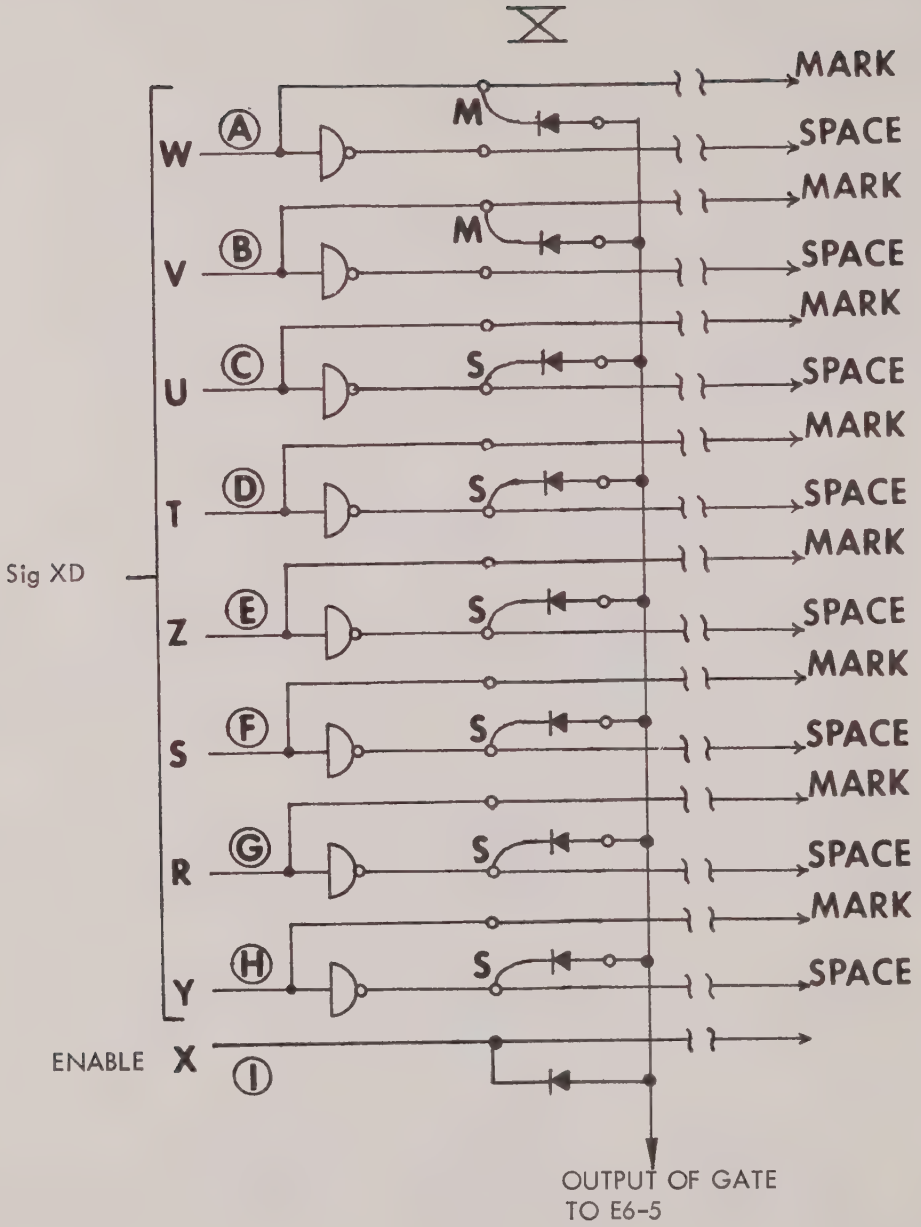


Figure 4-3. Character X Programmed for ETX (MMSSSSSS).
Note Even Parity is Used.

Inputs at the points labeled (A) through (I) are from the Signal Distributor. When a character has been entered into the shift register, the points (A) through (H) are either high or low depending on the entered character. Assume ETX is programmed (as shown) and ETX is entered in the shift register. Points (A) and (B) will be high; (C) through (H) low, which is inverted to a high where the diodes for bits 3 through 8 are programmed for SPACE. Inputs to the matrix diodes are now high; however, the gate enable at point (I) (CR20) remains low until the enable pulse is received from the Signal Distributor. The enable pulse is a L-H-L of about 250 microseconds. When it goes high, all inputs to the diodes are high. The inverter at E6-5 now has a high at its input and the output goes low. The low is then used to set a flip-flop.

4.2.3 Detector Circuits. Consist of flip-flops, inverters, and associated gates used to detect the programmed sequences. In turn, they activate the drive circuits. The following is an example of STX detection. See Figure 4-4.

Assume RSC has been received. On STX, the following sequence of events occurs:

(1) Input to STX inverter goes high.
(2) Output of STX inverter goes low.
(3) This low sets flip-flop; NL side high and NH side low. The NL side of the flip-flop is the inhibit to the selector magnet drive circuit. On STX the inhibit is released. The flip-flop sets NL to H. The NH side of the flip-flop allowed RSC before STX. On STX the NH side of the flip-flop goes low placing an inhibit on the RSC and TSC input gates. This keeps the selector from recognizing a programmed sequence that might appear in the text. To reset the flip-flop, EOT is detected, inverted through the EOT inverter to a low which resets the flip-flop to its quiescent condition.

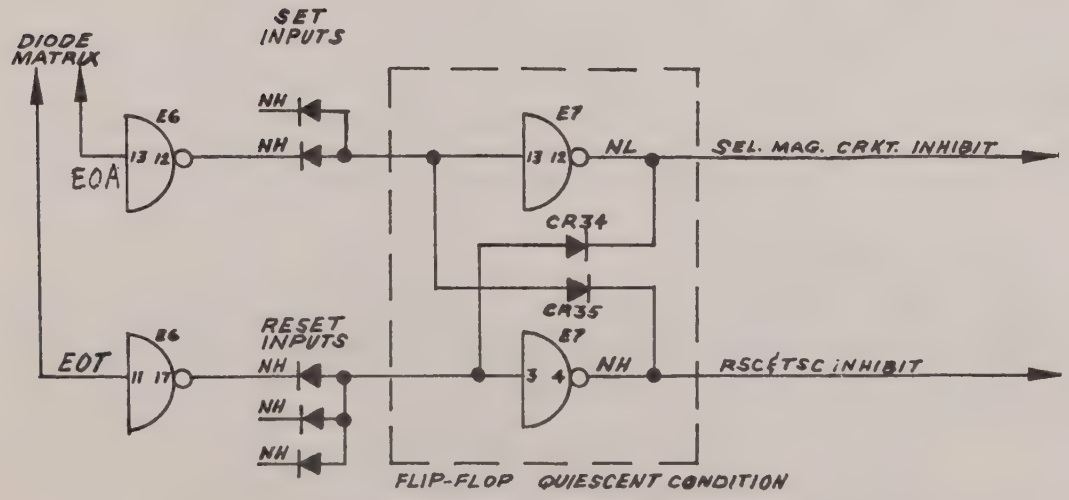


Figure 4-4. STX Detection Circuit

4.2.4 Drive Circuits. Drive circuits are used to actuate logic or control relays, provide time delay, reset sequences, drive answerback circuits and drive alarm lamps. For example — assume a station RSC has been received, then the drive circuit for activating the printers' motor control relay would be as shown in Figure 4-5.

On detection of the RSC, the input to the control flip-flop goes low and the output goes high allowing Q14 to go low pulling in the control relay K. The motor would remain on until EOT resets the flip-flop.

The preceding paragraphs give in a general way the operation of the various sections of the 8-Level Function #2 P.C. board. More detailed analyses of TSC, RSC and similar functions are given in the following paragraphs. Details of strapping options are presented in Section 3.

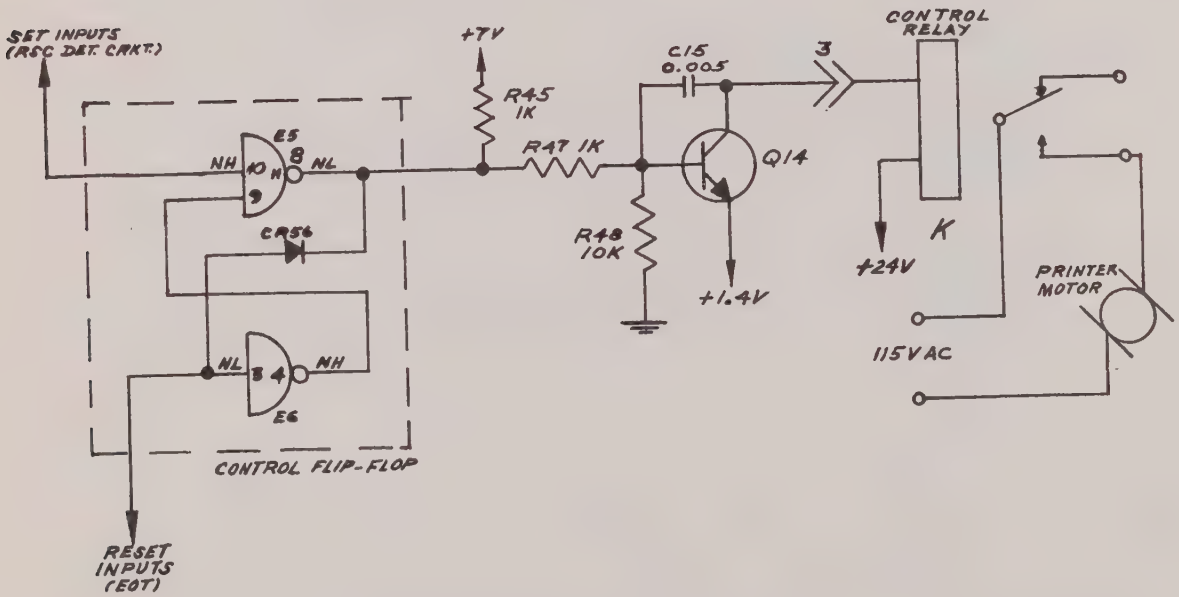


Figure 4-5. Relay Drive Circuit

4.3 Detailed Circuit Description

4.3.1 General. The detailed circuit description is keyed to the functional description, the simplified schematics and to the schematic diagram, Drawing E200407. Certain important circuit elements will be described. The major function flip-flops are:

SOH	E7/12, E7/4
INT	E7/6, E7/2
1st TSC	E4/11, E4/8
2nd TSC	E5/3, E7/8

1st RSC	E4/3, E4/6
2nd RSC	E5/8, E6/4
Broadcast	E5/11, E6/2
Emergency Stop	E3/10, E3/8

Jumpers 7, 8, 9 and 10 are used to feed through a signal for SOH, EOT, INT, and ETX respectively. The inverters for these functions are fed by diode matrix rows VII, VIII, IX, and X. The full matrix usage is:

Row	Function
I	2nd TSC
II	2nd RSC
III	Broadcast
IV	Emergency Stop
V	1st TSC
VI	1st RSC
VII	STX
VIII	EOT
IX	INT
X	ETX

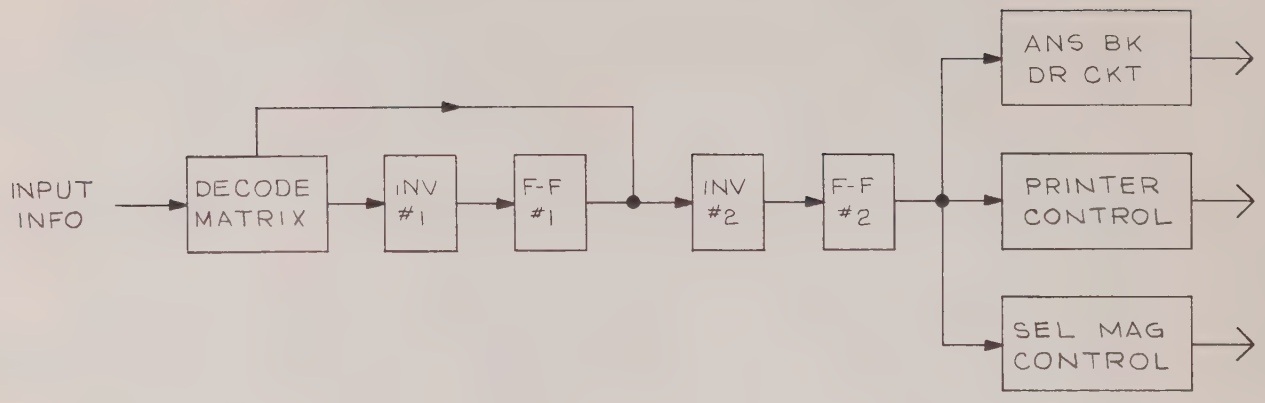
There are two flip-flops that are now shown on the functional block diagram. The broadcast flip-flop, E5/11 — E6/2, and the emergency stop flip-flop, E3/10 — E3/8. The broadcast flip-flop functions in the same manner as the 2nd RSC flip-flop. This circuit allows the processor to address a group of stations without consuming the time required for individual addressing. However, individual answerbacks are not possible in response to a broadcast request. Usually, one station will answerback for all stations. The answering station (usually last in the polling sequence) will have its AB strap made (near CR58).

The alarm flip-flop, E3/10 — E3/8, is normally used to recognize abnormal situations. For example: If diode CR1 is present and jumper AL is made, the reception of an interrupt followed by a character IV from the matrix would set the flip-flop and turn on driver Q1. The driver could be used to energize an emergency stop relay. Note that the character IV does not have to directly follow interrupt. This space allows the interjection of a service message before the station is locked out.

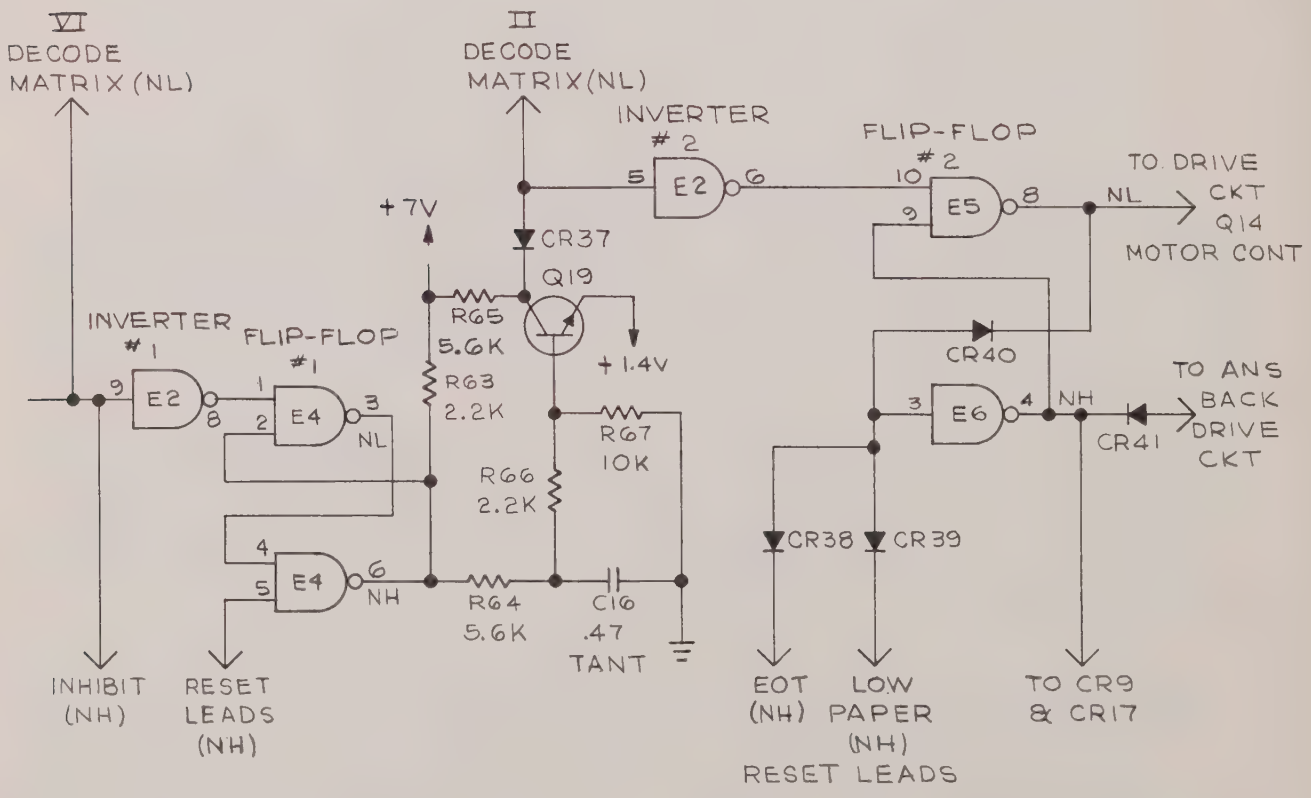
The alarm flip-flop can also be set from within the station by placing a low (or common) on input pin 9. This path might be used if an emergency situation developed at the station, such as a tight tape, running out of paper, or any other unusual condition.

4.3.2 RSC Detection. Figure 4-6, detail A is a flow chart showing the RSC detection sequence. Detail B shows schematically the circuit from Inverter #1 to flip-flop #2.

The decode matrix puts out a high (enable) as discussed in paragraph 4.2.2. The matrix may be considered as the enable/disable of a sequence of events we wish to send from left to right. Characters VI and II in the matrix must be received in succession. Assume reception of the two programmed characters in sequence. The events would be as follows:



A. FLOW CHART OF RSC DETECTION CIRCUIT



B. SCHEMATIC OF RSC DETECTION CIRCUIT

Figure 4-6. RSC Detection Circuit

a. The input to Inverter #1 at E2-9 goes high, E2-8 goes low, flip-flop #1 sets (i.e., E4-3 high, E4-6 low), E2-9 remains high during the enable pulse to the decode matrix. This enable is a high-low-high of about 250 microseconds. Approximately 100 microseconds after the enable, the reset lead to flip-flop #1 goes high-low-high (about 50 microseconds duration) before the enable is removed. This is the READ pulse. The read pulse is generated once per character. Since the inputs to the flip-flop are now low at E4-1, -2 the read pulse cannot reset the flip-flop during this character. The low at E4-6 turns off transistor Q19 to allow an open gate at CR37 and allow recognition 2nd RSC at E2-5. The decode matrix goes high, Inverter #2 goes low at E2-6 setting flip-flop #2. The read pulse during the second character resets flip-flop #1. Flip-flop #2 remains set until EOT.

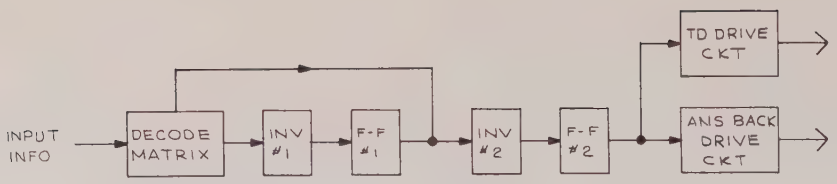
b. The Broadcast RSC is received in the same manner except that the sequence is VI and III. The inverter and flip-flop for Broadcast RSC detection appear on the schematic just below the station RSC circuitry. Normally, only one station, usually the last one of the polling sequence, is programmed for answerback. It is programmed at the point labeled AB on the schematic.

c. When flip-flop #2 is set, three functions are performed:

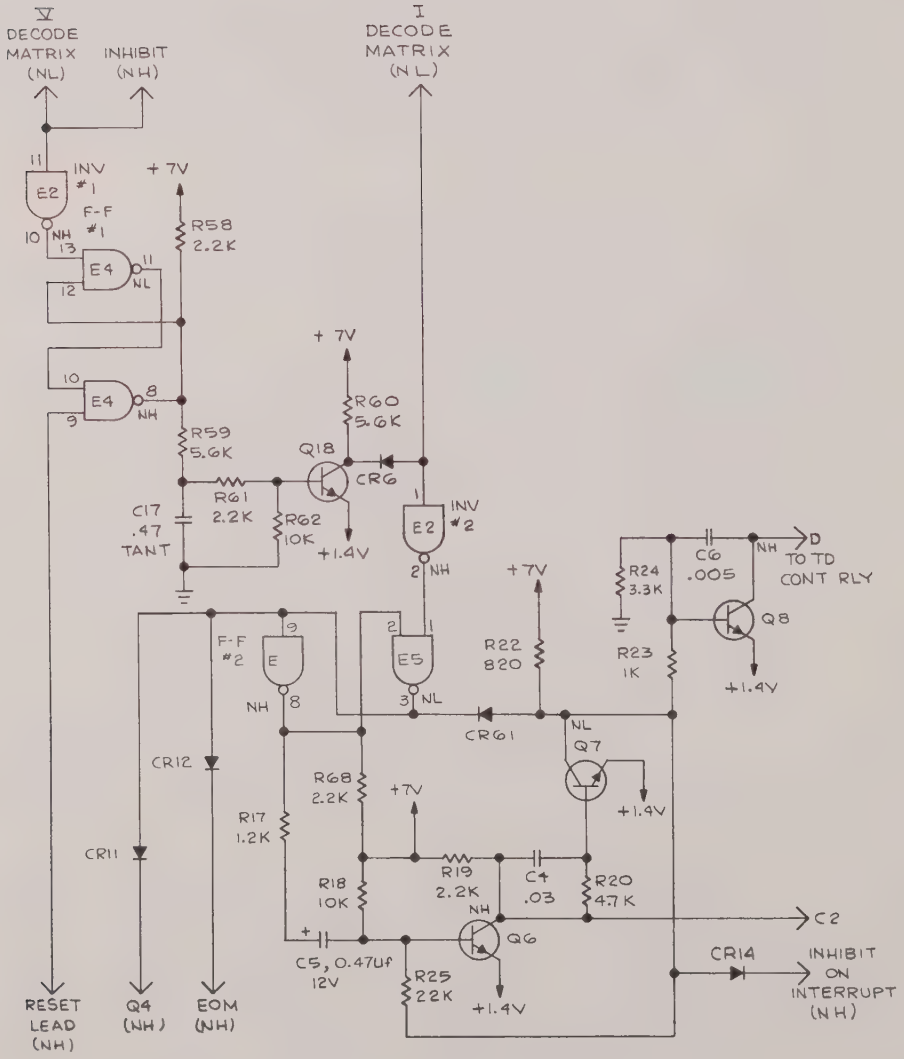
(1) NL side goes high: This causes Q14 to go low energizing the motor control relay to the printer.
(2) NH side goes low:
   (a) Pulses answerback drive circuit as follows:
   Transistor Q10 goes NL-H-L causing Q11, NH-L-H.
   Q11 causes Q12, NH-L-H causing Q13, NL-H-L.
   Q13 output activates the answerback program circuit on the Signal Distributor. Pulse width at Q13 is about 30 microseconds.
   (b) Low applied through CR17 to E7-11 is inverted to a high at E7-10. The high is fed to the selector magnet control gate (E9-13 on Signal Distributor) enabling the gate to be modulated through CR30.

4.3.3 TSC Detection. Figure 4-7, detail A is a flow chart showing the TSC detection sequence. Detail B shows schematically the circuit from Inverter #1 to the drive circuit. Detection sequence for TSC is basically the same as for RSC detection.

Detection of TSC occurs as outlined for RSC detection except that the two successive characters are V and I instead of VI and II. Under quiescent conditions Q6 is NL and Q8 NH. Transistor Q7 is kept low at its collector by the low from flip-flop #2 at E5-3 through CR61. When flip-flop #2 sets, CR61 goes back biased. Transistor Q6 goes NL-H-L. With Q6 high, Q7 is held low but as Q6 starts low again it causes Q7 to go high. The feed back resistor R25 is used to speed up the turn off of Q7. As Q7 goes high, Q8 goes low. If there is no tape in the gate, Q8 does not have time to pull in the control relays since when Q6 goes low through C2, it causes Q3 high in turn causing Q4 low driving Q5 high and pulsing the answerback circuit and resetting flip-flop #2 at CR11. If there is tape in the gate a low from the Tape Reader Card through CR7 (pin 7) clamps Q3 low disabling the answerback drive circuit. This allows Q8 to energize the control relay closing the circuit to the TD clutch. When ETX is read on the tape, a momentary low is applied to pin L from the Tape Reader. This pulse is fed through CR43 resetting flip-flop



A. FLOW CHART OF TSC DETECTION CIRCUIT



B. SCHEMATIC OF TSC DETECTION CIRCUIT

Figure 4-7. TSC Detection Circuit

#2 restarting tape idle. The selector will now wait for the computer to poll again and restart the TD. If it is the last message on the tape, the tape idles until the TD Control Circuits have opened. If tape out or tight tape occurs before ETX , the Tape Out and Initiate relays are de-energized and a low applied on pin M through C10 and CR42 resetting flip-flop #2.

4.3.4 Interrupt Detection. Full-duplex only. If the station is sending or receiving, the computer will interrupt (poll) the station by sending an INT character. The decode matrix detects the character and sets the Interrupt flip-flop. Setting of the flip-flop performs three functions, they are;

a. Inhibit printer
b. Inhibit TD
c. Enable the ETX character.

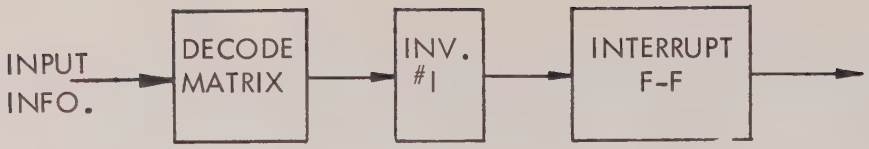
Figure 4-8, detail A is a flow chart showing the Interrupt Detection circuit. Detail B shows schematically the circuit from Inverter #1 to the Interrupt flip-flop.

On detection of INT, E6-9 goes high and E6-8 low. The low sets the Interrupt flip-flop E7-6 high, -2 low. The high at -6 enables the Decode Matrix E2-13 at CR1. The low at E7-2 is fed through CR14 (provided strap 12 is made) disabling Q8 which de-energizes the TD control relay and through CR19 to the Signal Distributor (provided strap C-1 is made) disabling the selector magnet control gate. To resume operation, the computer sends STX to reset the Interrupt flip-flop.

4.3.5 Emergency Stop Detection. The computer will send INT — IV (emergency stop) to halt operation. INT is detected as discussed in paragraph 4.3.4. Emergency Stop (character IV) detection is allowed only after INT is detected. Figure 4-9, detail A is a flow chart showing the Emergency Stop Detection sequence. Detail B shows schematically the circuit from Inverter #2 to the Alarm Drive circuit.

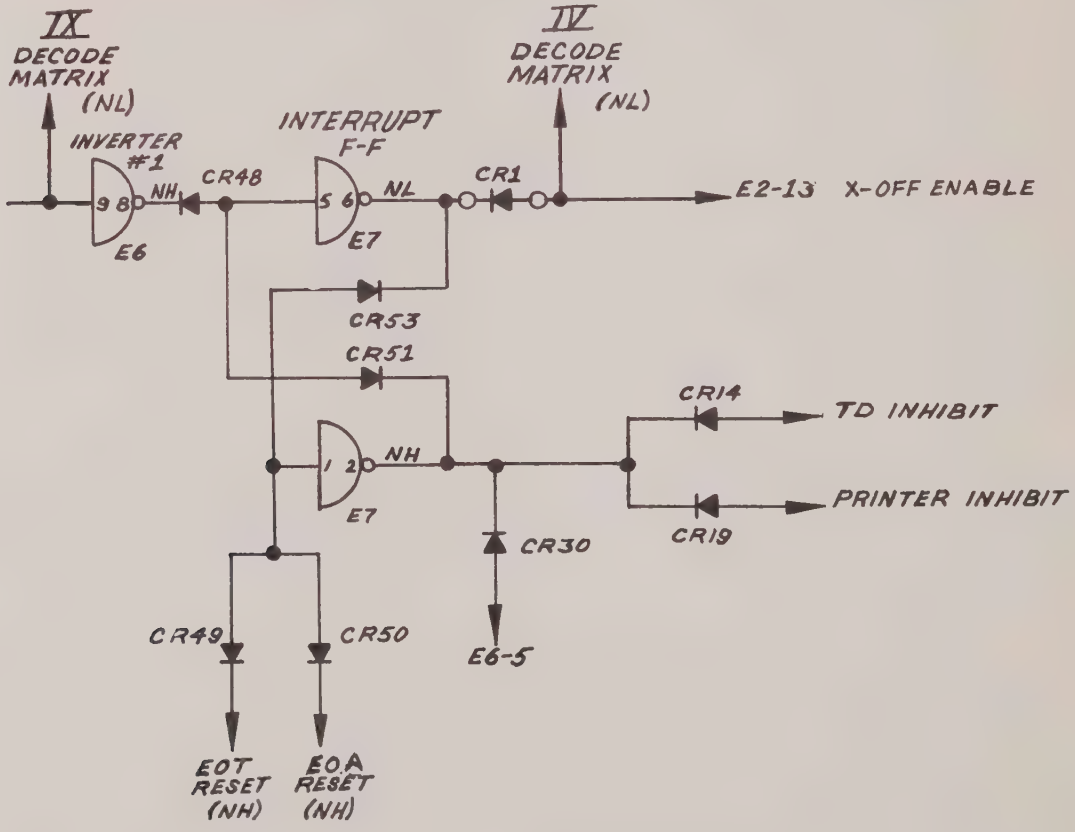
Emergency Stop assumes the TD is operating, otherwise flip-flop #2 will inhibit INT — IV (emergency stop) from being detected by a low from E5-3 through CR2 to E2-13. Assume flip-flop #2 is set. INT sets the Interrupt flip-flop enabling the Decode Matrix at IV by back biasing CR1. When IV (emergency stop) is detected, E2-13 goes high and -12 low. The low sets flip-flop #2, E3-10 high, -8 low. The high at -10 enables Q1 low energizing the Xmit Alarm Relay. The Read Pulse at CR5 does not reset flip-flop #3 during the IV character because E2-12 remains low while the Read Pulse is generated (refer to paragraph 4.3.2a). On the next character, flip-flop #3 is reset at the read pulse time but the Xmit Alarm Relay remains energized by means of a self-latching set up. Transistor Q1 can also be enabledif the TD is operating and a lack of stop pulse is detected. Diodes CR3 and CR4 will have high inputs enabling Q1 low operating the Xmit Alarm Relay. To resume operation once the alarm relay has been activated, the operator must depress the Initiate button and the computer must re-poll. This requirement results because activating the Xmit Alarm Relay de-energizes the Tape Out and Initiate relays, if so equipped.

4.3.6 Miscellaneous Circuits. A brief description of the functions of several of the strapping options is given in the following text. Refer to Schematic Diagram, Drawing E200407.



A FLOW CHART OF INTERRUPT DETECTION SEQUENCE

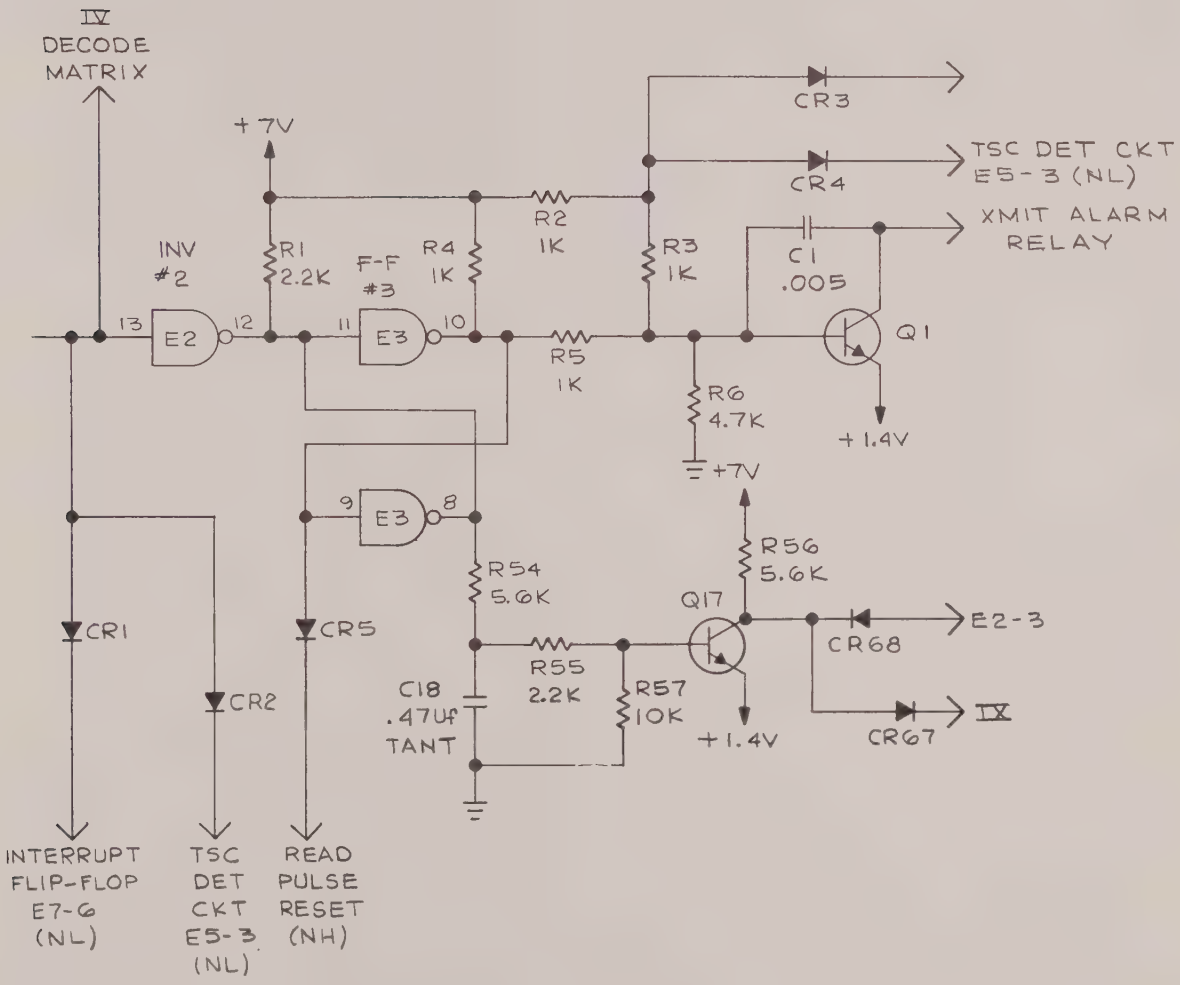
Schematically, the circuit from Inverter #1 up to and including the Interrupt f-f is as follows:



SCHEMATIC OF INTERRUPT DETECTION CIRCUIT

Figure 4-8. Interrupt Detection Circuit

A. FLOW CHART OF EMERGENCY DETECTION CIRCUIT



B. SCHEMATIC OF EMERGENCY DETECTION CIRCUIT

Figure 4-9. Emergency Stop Detection Circuit

a. To insure resetting of the Interrupt flip-flop after an Emergency Stop, strap 13 is made. INT resets the RSC, TSC inhibit flip-flop (with strap 11 made) establishing the RSC and TSC sequences but the Interrupt flip-flop will not be reset unless an EOA/SOM is received. If EOA/SOM is not received and it is required to enable the TD, the tape must be placed in the gate enabling Q2 high at E5-5. When a TSC is received, E2-2 goes low. This low is inverted through inverter E3-1, -2 to a high at E5-4. E5-6 goes low. This low is applied to the Interrupt flip-flop through CR52 resetting it.

b. It is possible by means of strap 6 to set the RSC and TSC inhibit flip-flop when tape is placed in the gate and a TSC received. This enables the printer and inhibits further RSC, TSC detection during text. Strap 6 is normally used only in half-duplex operation.

c. Strap 14 enables receiver for service message between alarm and EOT.

d. Straps 15 and 16 provide auxiliary driver bias.

5. ORDERING INFORMATION

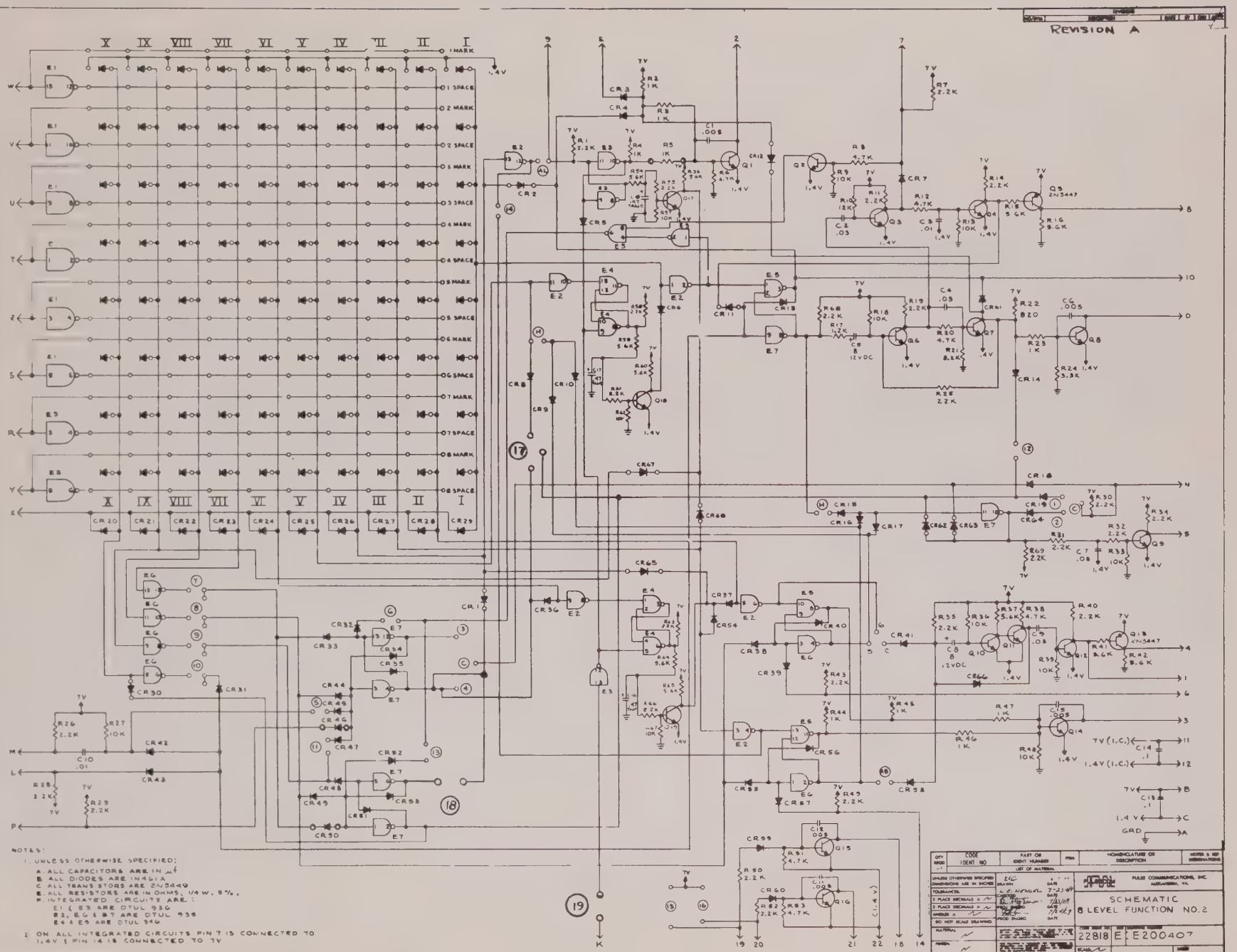
Order from:

Pulse Communications, Inc.
5714 Columbia Pike
Falls Church, Virginia
22041

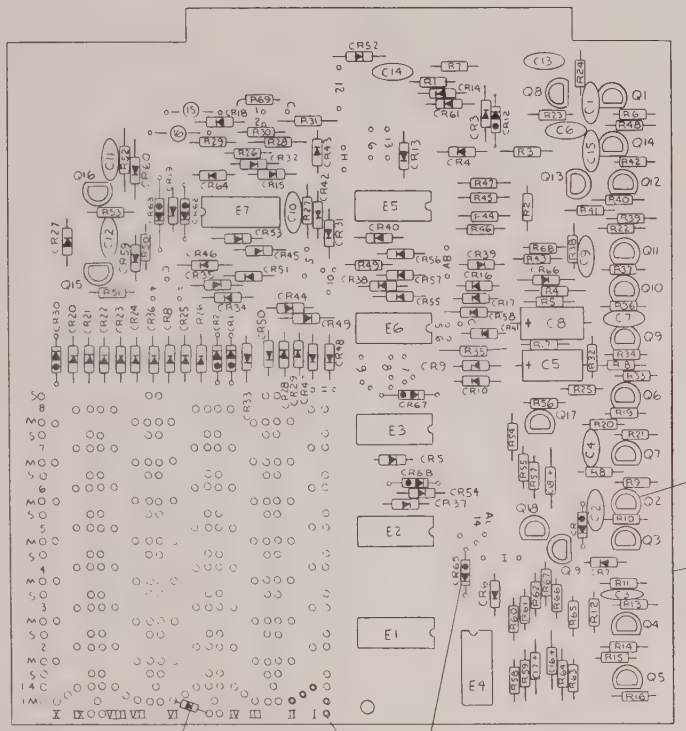
Telephone: 703/820-0652
Telex: 89-9423

6. DRAWINGS

D100408
E200407


REVISION A
NOTES:
1. UNLESS OTHERWISE SPECIFIED:
A. ALL CAPACITORS ARE IN μF
B. ALL DIODES ARE IN4614
C. ALL TRANSISTORS ARE 2N3640
D. ALL RESISTORS ARE IN OHMS, 1/4 W, 5%.
E. INTEGRATED CIRCUITS ARE:
E1 (E3 ARE DTUL 936
E2, E6 & E7 ARE DTUL 939
E4 & E5 ARE DTUL 946
2. ON ALL INTEGRATED CIRCUITS PIN 7 IS CONNECTED TO 1.4V (PIN 14 IS CONNECTED TO 7V
SCHEMATIC
8 LEVEL FUNCTION NO.2
PULSE COMMUNICATIONS, INC.
22818
E200407

REVISIONS					
NO/SYM	DESCRIPTION	DATE	BY	CHK	APPD



INSTRUCTION MANUAL

Parity Checker
Model D100321
Issue 1

IN#158
(7/69)

INSTRUCTION MANUAL

Parity Checker
Model D100321
Issue 1

TABLE OF CONTENTS

	PAGE
1. GENERAL	1
2. SPECIFICATIONS	1
3. ORDERING INFORMATION	2
4. CALIBRATION	2
5. MAINTENANCE	3
6. FACTORY SERVICE/SPARE PARTS	3
7. CIRCUIT DESCRIPTION	4

PARITY CHECKER

Model No. D100321

1. GENERAL

The Model No. D100321 Parity Checker has been designed to detect lost or added impulses during an eight-level telegraph transmission. This printed circuit assembly is used by plugging it into a PULSECOM solid state selector.

The Parity Checker receives eight-level characters in parallel form. If the character's parity is correct, the parity checker accepts the character and then transmits the character to the selector magnet in serial form. However, if the parity is not correct, a predetermined character is substituted for the bad character; then this substitute character is transmitted in serial form. This sequence occurs without hesitation between characters.

At the time of error detection, an alarm pulse occurs and a circuit is set to remember this alarm condition. Then, after the message is complete, the parity checker can be polled for an error condition. This polling causes the parity checker to set a preselected character into the register and then causes this character to be transmitted in serial form over the answer-back line. Should polling occur when no error has occurred, the normal answerback line will be activated for the duration of the polling signal.

2. SPECIFICATIONS

Parity checking: Odd or even

Speed: 74.2 and 110 baud

Distortion: 3% nominal, 6% maximum

Substitute signals: Any combination of marks and spaces may be substituted for a character in error, or used as the answerback character. The substitute and answerback characters are independently selectable.

Output drivers: Two independent drivers, each capable of driving a selector magnet. Also, an independent driver for answerback character transmission.

Alarms: A pulse alarm activates at the time of each error. A steady alarm is activated by the first error and remains active until the parity checker is polled.

Activation and polling: Parity checking may be activated through any of four separate lines. A poll-for-error signal may be sent into two input lines.

3. ORDERING INFORMATION

The Model No. D100321 Parity Checker can be strapped to check for either even or odd parity. When ordering a board, specify odd or even parity. To change parity in the field, refer to Paragraph 4.2 in the maintenance section of this manual. Address orders to:

Pulse Communications, Inc.
5714 Columbia Pike
Falls Church, Virginia 22041

Telephone No. 703/481-0652
Telex: 89-9423

4. CALIBRATION

4.1 Clock Adjustment - The Parity Checker has a clock source for use during character transmission. This clock must be accurately set to minimize distortion. A frequency counter must be used to assure proper operation. To calibrate the clock source, proceed as follows:

1. Jumper the emitter of Q4 to common. This can most easily be done by connecting between R14 (the end nearest the edge of the board) to the cathode of CR34 (the end nearest the edge of the board).

2. Using a frequency counter, observe the signal at the collector of Q6. Access to this point can be had at R16, the end away from the edge of the board.

3. If required, adjust R39 for a period between positive transition of 9.09 msec for 110 baud and 13.47 msec for 74.2 baud. Other baud rates may be set by dividing the baud into one. This yields the time in seconds between positive transition.

4.2 Parity Selection - The Model No. D100321 Parity Checker can be strapped to check either even or odd parity. To check even parity, jumper A to C; to check odd parity jumper B to C. The jumper points are shown in Figure 4.1.

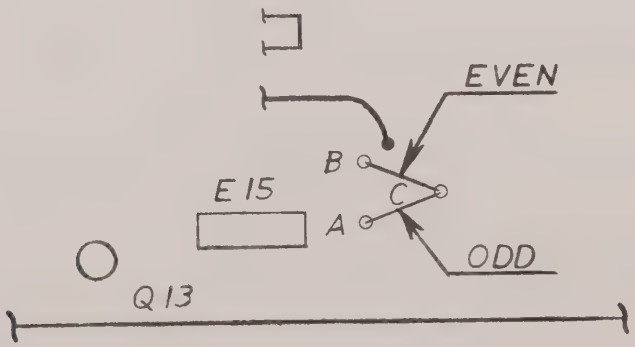


Figure 4.1

5. MAINTENANCE

5.1 General - There are no routine maintenance procedures required for the Model No. D100321 Parity Checker. However, if repairs are made, certain procedures should be used to accomplish the repairs, and after any component in the multivibrator circuit has been replaced, the calibration procedure must be performed.

When replacing a component part, care should be used to prevent overheating the board or the component. Use only enough heat to make a good solder joint. Also, when placing the component on the board, make a strain relief loop to avoid component damage. This is especially important for glass diodes.

5.2 Troubleshooting - Should trouble occur, the following procedure, using an oscilloscope, will usually help to isolate the failure.

1. Sync the oscilloscope on the positive sample pulse at pin X.

2. Check the clock pulses at the collector of Q6. The sample pulse will start the clock by setting the register.

3. If the clock does not start, look at E11 pin 11. This point should go to less than one volt when the register is set. If the clock does start, go to step 5.

4. If E11 pin 11 does not go negative, check the gates at E12 pin 8 and E12 pin G. One of the gates (depending on whether an error has occurred) should go low and set a space into the last register flip-flop, which puts a low on the cathode of CR31 to start the clock.

5. The entire character can be observed by syncing on the sample pulse (pin X) and looking at E5 pin 9. Adjust the oscilloscope time base to display one character width. Any missing bit may now be observed.

6. FACTORY SERVICE/SPARE PARTS

6.1 Factory Service - Prompt service can be obtained by returning the failing unit transportation prepaid to the factory. When the unit is shipped, the plug-in printed circuit boards should be unplugged and wrapped separately. Usually only the failing board need be shipped.

Include a purchase order describing the nature of the defect and the repairs authorized.

6.2 Spare Parts - When ordering spare parts or assemblies, describe by Model and Serial number of the equipment in which the spare parts or assemblies are to be used. Order all parts and assemblies by PULSECOM part number.

6.3 Ordering Address

Send order for both parts and service to:

Pulse Communications, Inc.
5714 Columbia Pike
Falls Church, Virginia 22041

Telephone No. 703/481-0652
Telex: 89-9423

7. CIRCUIT DESCRIPTION

Most of the circuitry on the parity checker board is housed in integrated circuit logic modules. However, there are a few discrete-component circuits. A description of these circuits will be given in the beginning paragraphs. Then the overall logic will be explained.

7.1 Clock Circuit - In order to allow parallel character input and serial character output, a shift register is used. The shift register requires a shift pulse source. In addition, the shifting rate sets the transmission rate. Thus, the rate of the shift pulse must be controlled. In the Parity Checker, a gated multivibrator is used as the clock source. Gating is required to control the time of the beginning of transmission.

Transistors Q4 and Q5 are connected to form the multivibrator clock. When the output at pin 4 of E12 is high, transistor Q4 will be at cut off because while its emitter will be at approximately +4 volts its base will be at approximately +1.4 volts (the drop across CR33 and CR34). At this time, transistor Q5 will be turned on to saturation because of the base current through R11. When the clock needs to be activated, E12 pin 4 will go to approximately +0.4 volt (it does not go completely to ground because of the voltage drop across its final transistor). The lowering of Q4's emitter will cause it to drive into saturation. The resulting collector current will cause a voltage drop across R10. The resulting negative voltage swing is coupled through C5 to the base of Q5, turning Q5 off. When Q5 turns off, positive pulse will couple through C6 to the base of Q4, but because Q4 is already on this has no effect. Capacitor C5 will discharge through R11, thus raising the base of Q5 above ground. When Q5 turns on again the collector current will cause a voltage drop across R13. This negative going transition is coupled through C6 to the base of Q4, and turns Q4 off. The collector of Q4 will now go positive until C6 discharges through R12 and potentiometer R39. The result is a square wave at the collector of Q4. The negative time duration is fixed by the time constant of C5, R10, and R11; the positive time duration is set by the time constant of C6, R12, R13, and potentiometer R39. This latter adjustment is available to allow variation of the baud as required.

The square wave at the collector of Q4 is fed through C7 and CR35 to the base of Q6. The negative transition will cause Q6 to cut off, placing a positive pulse on the collector,

which in turn is fed to the clock inputs of the shift register flip-flops. Capacitor C7 will discharge through R14. This sets the duration of the positive impulse (transistor Q6's cut off time).

7.2 Pulse Alarm One-Shot - When an error is detected, a ground pulse is sent over the pulse alarm output line (pin D). This pulse is generated by activating the one-shot made up of Q7 and Q8. When no error is preset, transistor Q8 will be in saturation because of the base current through R19. This causes the collector of Q8 to be nearly down to ground, holding Q7 and output transistor Q9 at cut off. When an error occurs, the collector of Q7 will be momentarily grounded through CR37. This impulse is coupled through C10 to cut off Q8. When Q8 turns off its collector voltage goes positive, which turns Q7 on. At the same time, the collector of Q8 going positive will turn Q9 on to ground the pulse alarm output line. Transistor Q8 will hold the pulse on until C10 discharges through R19 to turn on Q8, and cut off Q7 and Q9. The pulse duration is controlled by the time constant of C10 and R19. For another pulse to occur, the collector of Q7 must go positive, then negative.

7.3 Logic Description - Flip-flop E15 is used to count the number of pulses in a character. When the character is complete, the flip-flop will be returned to its initial state for even parity. For odd parity it will not finish in its initial state. The character is fed through pin 7 from the input relay. Pin 7 is at a high level for marking, low for spacing. The flip-flop is clocked by the input at pin H. Pin H is the 50% flip-flop from the distribution circuit. Each positive transition at pin H will cause a negative transition at E14 pin 2. This is coupled through C9 to the base of Q13, cutting it off and causing the clock input, pin 2, of the flip-flop to go positive. When the clock pulse goes negative, the flip-flop will change state if a mark is preset on pin 7.

When the complete character has been read into the distribution card, input X will go high to initiate the parity check and transmission of either the acceptable character or the substitution character.

The sample pulse (high) at pin X is applied to the cathode of diode CR39. This diode in combination with diodes CR36 and CR40, forms an AND circuit. If the cathode of CR36 is high at sample time and the cathode of CR40 (the enable diode) is also high, an error condition is indicated. This resulting high at pin 3 of E11 will cause the output at E11 pin 4 to go low. The inverter output at E11 pin 4 feeds four circuits. First, diode CR37 will start the pulse alarm output (refer to Paragraph 2.2). Second, lowering the input at E7 pin 1 will set the flip-flop E7-E7, and in turn this turns Q10 on to ground the alarm output line, pin 4. Third, diode CR1 inhibits reading the out of parity character into the register. Fourth, a low at E12 pin 1 causes the error substitution character to read into the register.

Characters are normally read into the register from the distributor circuit. However, if a character is found to be in error, a substitution character is used. When an answer back signal is received and an error has occurred, a second substitution character is placed in the register for transmission.

Normal character entry is from the data input pins. They are: bit 8 - pin Y, bit 7 - pin R, bit 6 - pin S, bit 5 - pin Z, bit 4 - pin T, bit 3 - pin U, bit 2 - pin V, and bit 1 - pin W. Each pin has an input inverter for line termination, level-setting, and buffering. At sample time, a high will appear at E12 pin 8 to gate the data through to the register (if no error has been detected). For example, if bit 8 is present input pin Y will be low. The resulting high conditions E6 pin 13 to pass bit 8 at sample time. When the sample pulse occurs E6 pin 11 will go high setting bit 8 into the register through E1 pin 4. The other bits operate in an identical fashion. However, if an error had occurred the cathode of CR1 would have been low at sample time, preventing the high at E12 pin 8 by clamping E11 pin 5 low. This same low causes the error substitution character to read into the register. The gating for the error substitution character is through E12 pin 1 (low), E12 pin L (high), E6 and E12 pin 5 (high), E6 and E12 pin 6 (low). Each register position entry point has a diode connected to this drive line. By clipping the diodes for the unwanted bits, a character may be selected. For example: If an A is wanted as the substitution character diodes CR18 and CR6 would be removed from the circuit, causing diodes CR4, CR8, CR10, CR12, CR14, CR16, CR20 to set an A into the register. Loading the register will cause the clock to run. If the cathode of any one of diodes CR23 through CR31 goes low as a result of a space being set into a bit position, the resulting low at E11 pin 11 will result in a low at E12 pin 4 and run the clock (for a detailed description of the clock, refer to Paragraph 2.1). The resulting clock pulses at the collector of Q6 are connected to the clock inputs of each register position. Register position E5 is set spacing at the initial register set time to insure starting the clock and to set the output line spacing.

Each clock pulse will shift the character one position to effect the serial transmission. The bit eight position has a continuous mark input. This results in the register going all marking at the last bit transmission to stop the clock.

The output from the register is taken at E5 pin 9 and applied to E10 pin 9 and E10 pin 13. During the transmission of a data or substitution character, E10 pin 10 will be conditioned with a high. This allows the character to pass to the base of Q1 and Q2 for selector magnet drive. However, during the transmission of an answer to an error condition poll, E10 pin 12 will have a high and E10 pin 10 will have a low. This results in the answerback character being transmitted over the answerback line through Q3.

At the end of a transmission in which an error occurred, an answerback polling signal on either pin E or pin 8 will cause the parity checker to transmit an answerback character. The polling signal (high) will turn Q11 on, which puts a low on E13 pin 1. The resulting high at E13 pin 2 will condition CR47 and CR50 to gate a signal. The flip-flop at E7 was previously set by an error. This flip-flop will now place a low on CR48 and a high on CR51. Because there is a high at both CR50 and CR51, transistor Q14 will turn on. When Q14 turns on, the low at its collector will set the answerback character into the register, reset the E10 flip-flop which gates the answerback line, and reset the error flip-flop at E7. When the collector of Q14 goes low, this transistion is coupled through C16. This pulse turns Q12 on momentarily to reset the error flip-flop at E7. The low at the collector of Q14 is also used to reset the answerback flip-flop at E10 pin 51. Finally it puts a low on the answerback-character diodes (CR5, 7, 9, 11, 13, 15, 17, and 19). This character sets into the shift register, which in turn

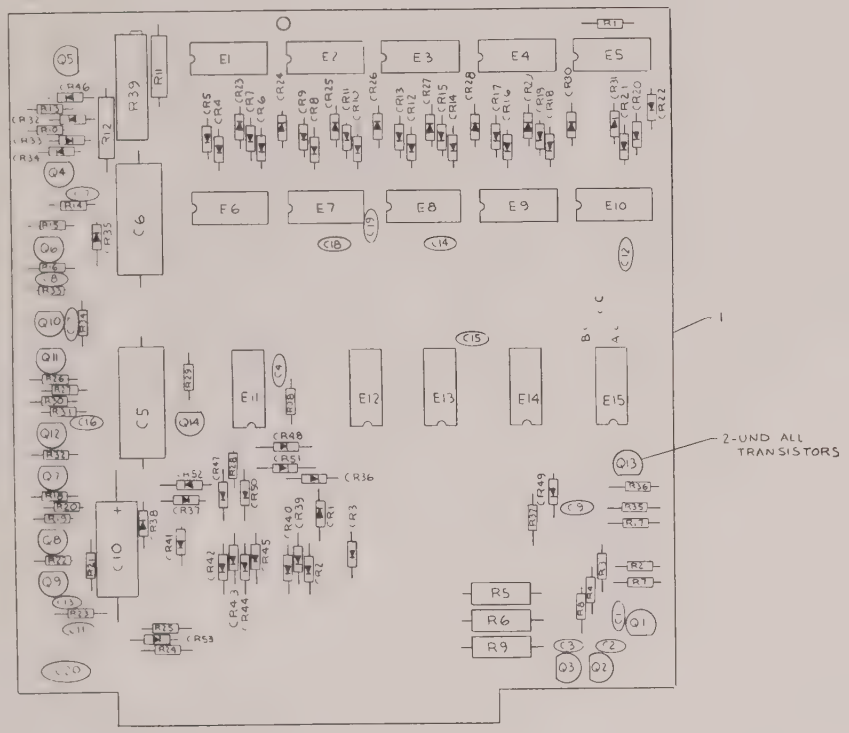
starts the clock and then the character is transmitted in the normal fashion. However, E5 pin 9 is now gated through E10 pin 13 by the high at E10 pin 12. This sends the character over the answerback line while blocking it from the selector magnet lines. The next time the distributor clock runs, pin F will go high. This will restore the E10 flip-flop and reset the bit counting error detection flip-flop E15.

In order for an error to be detected, the unit must be enabled. A high at E8 pin 3 gates errors through by conditioning the cathode of CR40. This same high also allows data to be gated into the parity checker by removing the clamp through CR2. A low on any or all of pins J, K, L, and M will condition the parity checks to detect errors. The appearance of a low at E11 pin 1 will cause a high at E11 pin 2, E14 pin 13, a low at E14 pin 12, and a high at E9 pin 6. Also, the high at E11 pin 2 will set a low at E9 pin 3. This will set the flip-flop at E8. If the low select signal remains, the flip-flop at E8 will remain set and parity errors will be detected. However, if the select is removed one additional character will be tested. The first sample pulse at pin X will cause the last character to be tested and will also reset the flip-flop to block further checking. Checking will be restored by the next select.

REVISIONS					
NO/SYM	DESCRIPTION	DATE	BY	CHK	APPD

ITEM	REF DESIGNATION
10	C1, C2, C3, C7, C11, C12, C13, C14, C15, C17, C18, C19
16	R1, R21, R24, R25, R26, R32, R36
21	R7, R8, R22, R23, R33, R34
25	R14, R19, R20, R27, R29
26	R15, R16, R17, R18, R28, R30, R31, R35, R37

NOTES:
1. EITHER 801-0461 OR B500034 MAY BE USED.



QTY REQD	CODE IDENT NUMBER	PART OR IDENT NUMBER	ITEM	NOMENCLATURE OR DESCRIPTION	NOTES & REF DESIGNATIONS
			31		
			30		
REF		D200347	29	SCHEMATIC	
1		742-1002	28	RESISTOR VAR 10K	R39
1		204-4709	27	RESISTOR 47Ω, 1/4W 5%	R38
9		204-2201	26	2.2K, 1/4W, 5%	SEE TABLE
5		204-1002	25	10K, 1/4W, 5%	SEE TABLE
1		753-1212	24	12.1K, 1/2W, 1%	R12
1		753-2212	23	22.1K, 1/2W, 1%	R11
2		204-1001	22	1K, 1/4W, 5%	R10, R13
6		204-1501	21	1.5K, 1/4W 5%	SEE TABLE
		202-6200	20	620Ω, 1W, 5%	R9
2		202-1200	19	120Ω, 1W, 5%	R5, R6
2		204-4700	18	470Ω, 1/4W, 5%	R3, R4
1		204-5600	17	560Ω, 1/4W, 5%	R2
7		204-5601	16	RESISTOR 5.6K, 1/4W 5%	SEE TABLE
		3403-9102	15	CAPACITOR .1 uf	C20
1		3340-0350	14	35 uf	C10
2		3404-0202	13	.002 uf	C8, C9
2		3316-9682	12	.68 uf	C5, C6
2		3403-9103	11	.01 uf	C4, C16
2		3403-0502	10	CAPACITOR .005 uf	SEE TABLE
1		700-0935	9	INT CIRCUIT	E11
3		700-0936	8	INT CIRCUIT	E12, E13, E14
5		700-0946	7	INT CIRCUIT	E6 THRU E10
4		700-9099	6	INT CIRCUIT	E1 THRU E4
2		700-0945	5	INT CIRCUIT	E5, E15
53		SEE NOTE 1	4	DIODE	CR1 THRU CR53
14		904-3704	3	TRANSISTOR	Q1 THRU Q14
14		82-0002	2	PAD, TRANSISTOR	
1		D501324	1	BD, PRINTED CIRCUIT	

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES:
2 PLACE DECIMALS ± —
3 PLACE DECIMALS ± —
ANGLES ±
DO NOT SCALE DRAWING
MATERIAL: —
FINISH: —

DRAWN: W. GLEADALL 7 FEB 69
CHECKED: 4-17-69
PROJ. ENGRG: 4/18/69
PROD ENGRG: 4-18-69

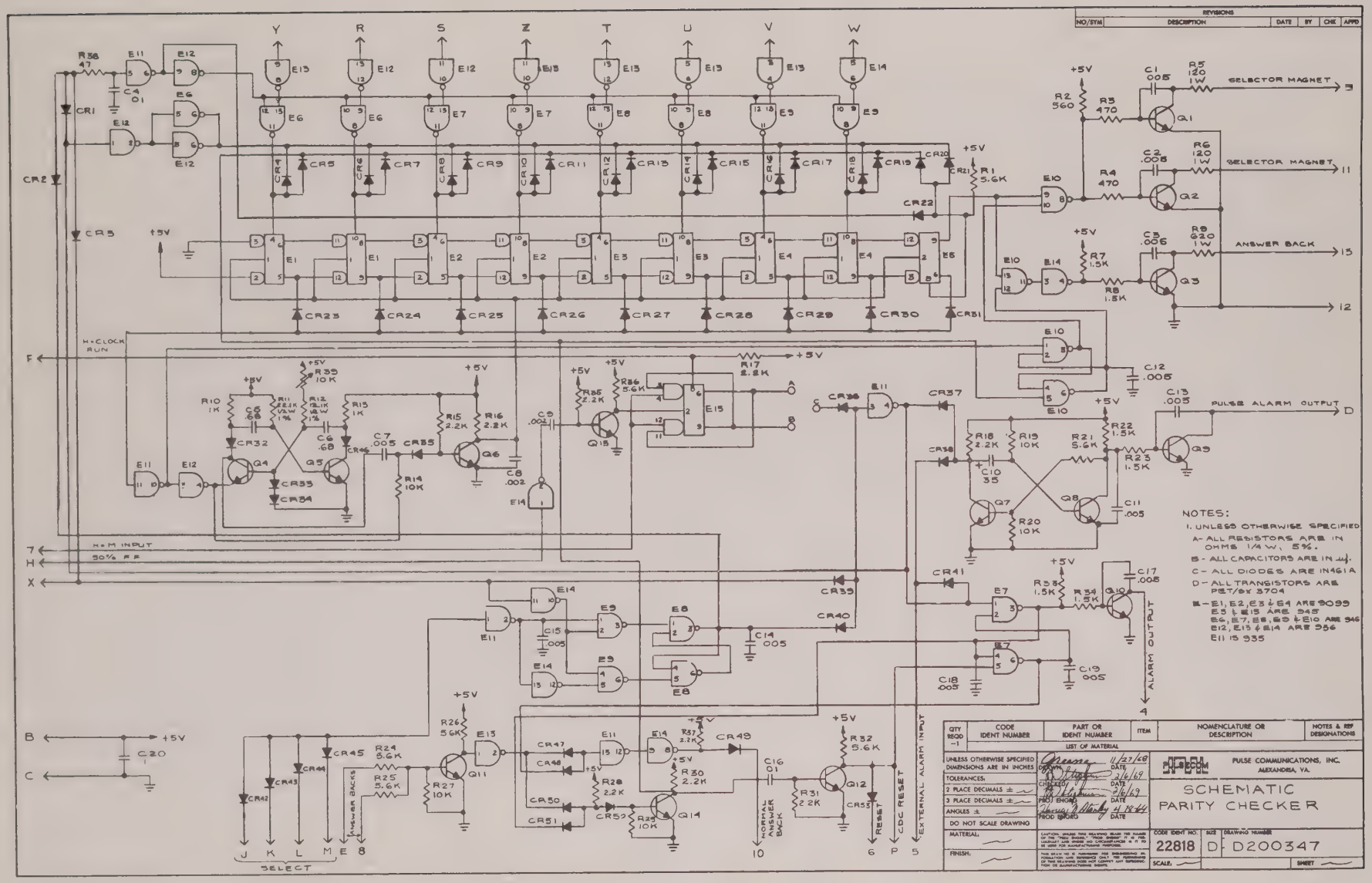
CAUTION: UNLESS THIS DRAWING BEARS THE NAME OF THE "PROD. ENGRG." THEN SHOWN IT IS FOR LIABILITY AND ORDER NO CIRCUMSTANCES IS IT TO BE USED FOR MANUFACTURING PURPOSES.

THIS DRAWING IS FURNISHED FOR INFORMATION OR INSTALLATION AND REFERENCE ONLY. THE FURNISHING OF THIS DRAWING DOES NOT CONVEY ANY LICENSE TO USE OR MANUFACTURING RIGHTS.

PULSECOM — PULSE COMMUNICATIONS, INC. ALEXANDRIA, VA.

BOARD, P.C. ASSY PARITY CHECKER

CODE IDENT NO. 22818 | SIZE D | DRAWING NUMBER D100321 | SCALE: 2/1 | SHEET



NOTES:

1. UNLESS OTHERWISE SPECIFIED
   - A- ALL RESISTORS ARE IN OHMS 1/4 W, 5%.
   - B- ALL CAPACITORS ARE IN μf.
   - C- ALL DIODES ARE IN461A
   - D- ALL TRANSISTORS ARE PET/DX 3704
   - E- E1, E2, E3 & E4 ARE 9099 E5 & E13 ARE 945 E6, E7, E8, E9 & E10 ARE 946 E12, E15 & E14 ARE 956 E11 IS 935

REVISIONS

NO/SYM	DESCRIPTION	DATE	BY	CHK	APPD

LIST OF MATERIAL

QTY REQD	CODE IDENT NUMBER	PART OR IDENT NUMBER	ITEM	NOMENCLATURE OR DESCRIPTION	NOTES & REF DESIGNATIONS
-1					

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES:
2 PLACE DECIMALS ±
3 PLACE DECIMALS ±
ANGLES ±
DO NOT SCALE DRAWING
MATERIAL
FINISH

DRAWN 11/27/68
CHECKED 2/6/69
PROJ ENGNG 2/6/69
PROD ENGNG 4/18/69

PULSE COMMUNICATIONS, INC. ALEXANDRIA, VA.

SCHEMATIC PARITY CHECKER

CODE IDENT NO. 22818 | SIZE D | DRAWING NUMBER D200347

SCALE: | SHEET

PULSECOM

PULSE COMMUNICATIONS, INC.

INSTRUCTION MANUAL

Multi-Level Signal Distributor
Model D501377
Issue 1

IN#125
(3/69)

5714 COLUMBIA PIKE, FALLS CHURCH, VIRGINIA 22041 • TELEPHONE 703/481-0652 • TELEX 89-9423

INSTRUCTION MANUAL

Multi-Level Signal Distributor
Model D501377
Issue 1

IN#125
(3/69)

TABLE OF CONTENTS

	PAGE
1. GENERAL	1
2. SPECIFICATIONS	1
3. MOUNTING	3
4. ORDERING INFORMATION	3
5. INSTALLATION	5
6. CALIBRATION	9
7. CIRCUIT DESCRIPTION	13
8. MAINTENANCE	19

Multi-Level Signal Distributor
Model D501377

1. GENERAL

1.1 The Multi-Level Signal Distributor is one of the selector series logic cards used in code sequence recognition systems. It can be programmed to operate in five, six, seven or eight level systems.

1.2 Information in serial form is fed from the telegraph loop to the Signal Distributor. The Signal Distributor presents it in parallel form to a decoder. For answer back applications, it is capable for accepting information in parallel form and shifting it out in serial form. Interfacing can be through a DC isolating mercury relay or a standard EIA input.

1.3 An internal clock provides the time base for the desired operating speed. A built-in calibrate circuit allows the operator to adjust the clock without the aid of a counter or oscilloscope.

1.4 A circuit, called a Lack of Stop Pulse Detector, provides an output for driving a remote alarm when the input loop goes open for a period exceeding one character.

1.5 Two circuits for driving the selector magnets or selector magnet drivers of associated teleprinters or reperforators are provided. In the event of an open circuit the drive circuits are locked for the duration of the open. This prevents the printers or reperfs from running open.

1.6 Four different circuits are available for programming answer back characters. Two are permanently wired in and two are available as strapping options. Single or double character answer back(s) are available depending on the logic used to select the program circuits and the strapping options used.

2. SPECIFICATIONS

- Voltage Requirements: +7V and +1.4 (used as reference)
- Logic Levels:
  a. Binary 1 (high): +5V nominal (greater than +2.5V above reference).
  b. Binary 0 (low): OV nominal (less than +1 V above reference).

5714 COLUMBIA PIKE, FALLS CHURCH, VIRGINIA 22041 • TELEPHONE 703/481-0652 • TELEX 89-9423

- Code Level: 5, 6, 7 or 8 level start/stop. Stop element must be of a unit length or longer.

- Modulation rate: Internal oscillator may be adjusted to operate at any desired speed. A built in calibrate circuit is provided. Accuracy of the oscillator is $\pm 1/2\%$ when set using the electronic counter method. Oscillator test point is readily accessible for ease in calibrating.

- Decode Enable Pulse: (L-H-L) Enables the gates on the decoder for readout to memory on the read pulse.

- Read Pulse: Internally generated pulse (L-H-L) causes decoded characters to be shifted into memory on the Universal Sequencer during the stop pulse of each character. A built in time delay ensures that the register is full before generating the read pulse.

- Acceptable Input Distortion:
  5 Level -- 45%
  6 Level -- 44%
  7 Level -- 43%
  8 Level -- 42%

- Lack of Stop Pulse Detection: The lack of Stop Pulse Detector detects open periods in excess of one character and provides a low for actuating remote alarms or controls. Activation of the circuit also causes the selector magnet circuits to go marking thus ensuring that the machines do not run open.

- Answer Back(s): Four different circuits are available for programming answer back characters. Two are permanently wired in and two are available as strapping options. Single or double character answer back(s) are available depending on the logic used to select the program circuits and the strapping options used. The program circuit codes the shift register with the programmed character; the character is then shifted out on line. During the answer back, the input to the shift register and the associated teleprinter(s) are inhibited.

• Selector Magnet Driver(s):	Two selector magnet drive circuits are provided. Both can drive a selector magnet or selector magnet drive circuit directly. Internal power supply can furnish up to 60 ma (max). That is, the combined current drain from both drivers should not exceed 60 ma.
• Temperature Range:	Operating: 0 to +55°C

3. MOUNTING

3.1 When purchased as a part of an overall selector assembly, the Multi-Level Signal Distributor mounts in the selector chassis in the position provided.

4. ORDERING INFORMATION

4.1 At time of order, specify the following:

a. Code level of operation.
b. Speed (baud) of operation.
c. Selector will drive: 1) Two selector magnets
*2) One selector magnet and one selector magnet drive circuit
3) Two selector magnet drive circuits
4) None

*If Sig XD is a replacement board, specify which output (Q3 or Q12) is to drive which circuit.

d. Answer back characters:
(1) Character A:_____ and 2nd Character_____ C or D
or
(2) Character B:_____ and 2nd Character_____ C or D

4.2 Order from:

Pulse Communications, Inc.
5714 Columbia Pike
Falls Church, Virginia 22041

Phone: 703/481-0652
Telex: 89-9423

5. INSTALLATION

5.1 The Multi-Level Signal Distributor mounts in the slot provided in the selector chassis. It mates to a 44 pin (22 pin double sided) PC edge connector, Cinch Mfg. Co. #251-22-30-160 or equivalent. Refer to paragraph 5.2 for a list of the PC pin connections and the functions of each point.

5.2

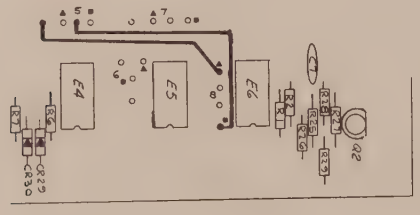
PIN#	FUNCTION
1	STOP bit output (NL)
2	Open
3	Open
4	External control lead (NH) for controlling Q3, magnet driver 1
5	External control lead (NH) for controlling Q12, magnet driver 2
6	External reset lead for resetting the parity check card
7	Clock pulses for parity check card
8	STOP bit output (NH)
9	Q10 output (NL); Read Pulse (NL-H-L) for reading decoded characters into memory.
10	Output lead for programming an external answer back card
11	External control lead (NL) for controlling Q14 (NH), one of the answer back programmers (at "B")
12	Output lead for programming an external answer back card
13	External control lead (NL) for controlling Q13 (NH), one of the answer back programmers (at "A")
14	Bit 7 output (NH)
15	Bit 6 output (NH)
16	Bit 4 output (NH)
17	Bit 3 output (NH)
18	Bit 2 output (NH)

PIN#	FUNCTION
19	Bit 1 output (NH)
20	Output (NL) pulse (called "enable pulse") for external use by the decode section of the 8 level function #1 card or other decoders
21	Bit 8 output (NH)
22	Bit 5 output (NH)
A	Circuit ground
B	+7V (V_{cc})
C	+1.4V (used as reference); Test Point (TP) 3
D	Output of Q12, magnet driver 2
E	Output of Q3, magnet driver 1
F	Output of Q11 (NH), Lack of Stop Pulse Detector
H	Shift register input (NH) from mercury relay; TP2
J	External control lead (NL) for controlling Q16 (NH); used to select the second answer back at "D"
K	Control lead (NL) for an external answer back
L	External control lead (NL) for controlling Q15 (NH); used to select the second answer back at "C"
M	Circuit ground
N	External program lead for Bit 8 (NH)
P	External program lead for Bit 7 (NH)
R	External program lead for Bit 6 (NH)
S	External program lead for Bit 5 (NH)
T	External program lead for Bit 4 (NH)
U	External program lead for Bit 3 (NH)

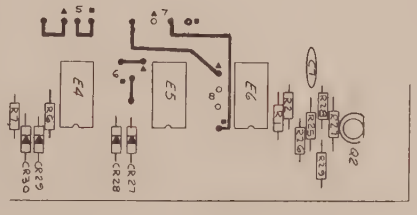
PIN#	FUNCTION
V	External program lead for Bit 2 (NH)
W	External program lead for Bit 1 (NH)
X	START bit output (NH); can be used as a decode enable
Y	Buffer flip-flop output (NH)
Z	Answer Back Relay Driver (NH)

(NOTE: Open pins are sometimes used as tie points or may be bussed thru)

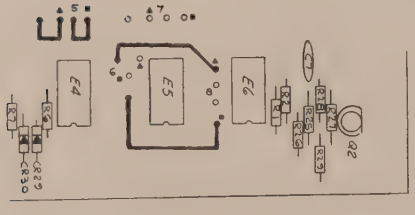
5.3 Programming the Multi-Level Signal Distributor shift register for 5, 6, 7 or 8 level operation is done as shown in Figure 5-1:



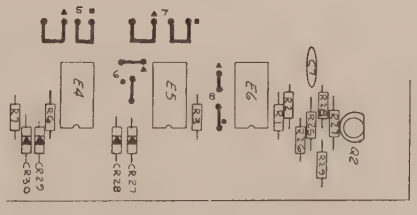
5 Level



7 Level



6 Level



8 Level

Figure 5-1

5.4 Answer back character programming. Four sets of diodes are provided on the PC board for programming answer back characters. See Figure 5-2. (See next page)

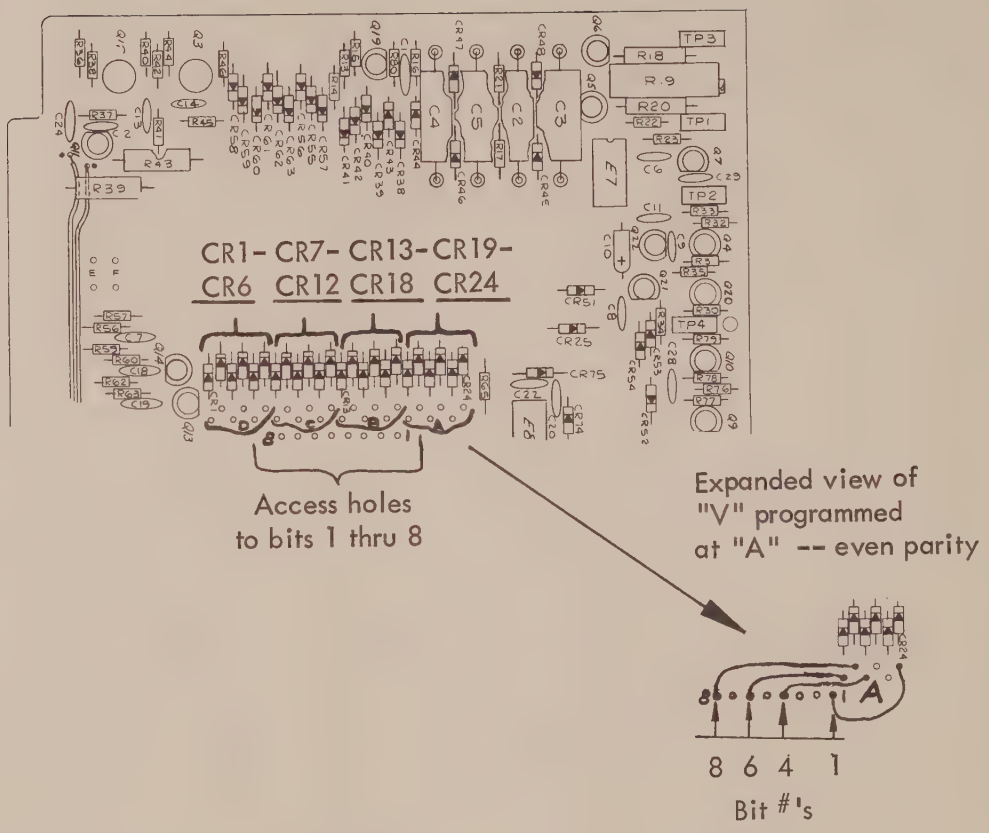
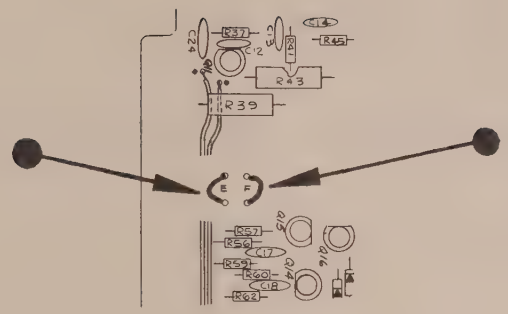


Figure 5-2

There are four sets of six diodes. Point "A" is associated with diodes CR19 thru CR24; point "B" with diodes CR13 thru CR18; point "C" with CR7 thru CR12; point "D" with CR1 thru CR6. The eight bits are accessible at the eight holes labeled 1 thru 8. 1 represents bit 1, 2 bit 2 etc. Determine what the answer back character(s) is (are) to be. Marks are automatically programmed. To program a space for a particular bit, connect the anode of one of the diodes in the group being used, to the hole (1 thru 8) for that bit. For example: To program a "V" answer back in eight level operation, say for group "A", connect the anode of any one of the diodes in that group to hole number 1, another to hole number 4, another to hole number 6 and another to hole number 8. Whenever Q13 is activated, it will program a space into bits 1, 4, 6 and 8. The eight bits (flip-flops) of the register can also be programmed from an external source. They are accessible from the PC edge connector, pins W, V, U, T, S, R, P, and N respectively. A group of diodes similar to the groups provided on the board should be used. A low of about 50 to 100 microseconds applied to their cathodes should be sufficient to set the connected bit. Be sure to remove any programming done at the factory to be sure that internal programming will not interfere with the external programming. If parity is not required, no diode is needed for bit #8.

5.5 Second character answer back programming. The second character answer back is programmed in the same manner as the first character at point "C" or point "D". Additional strapping is required at the points labeled "E" or "F". See Figure 5-3. (See next page). Refer to section 7. CIRCUIT DESCRIPTION paragraph 7.13 for a description of how the program circuits operate.

Strap point "E" to initiate the 2nd answer back character at Q16



Strap point "F" to initiate the 2nd answer back character at Q15

Figure 5-3

6. CALIBRATION

6.1 The internal time base (oscillator) can be calibrated by one of the following methods:

a. Using the built-in calibrate circuit.
b. Using an electronic counter.
c. Using an oscilloscope.

6.2 The operator will need a small screwdriver to adjust a Bourns trim-pot. If an electronic measuring instrument (VTVM, scope etc.) is used, the reference lead should be floating (isolated from ground). If it is not, then the reference lead should be connected to chassis ground and NOT to the test point listed. A "cheater plug" can be used to isolate the test instrument from ac ground.

6.3 Refer to Figure 6-1 for the location of the test points, components, etc. called out in the text. (See next page)

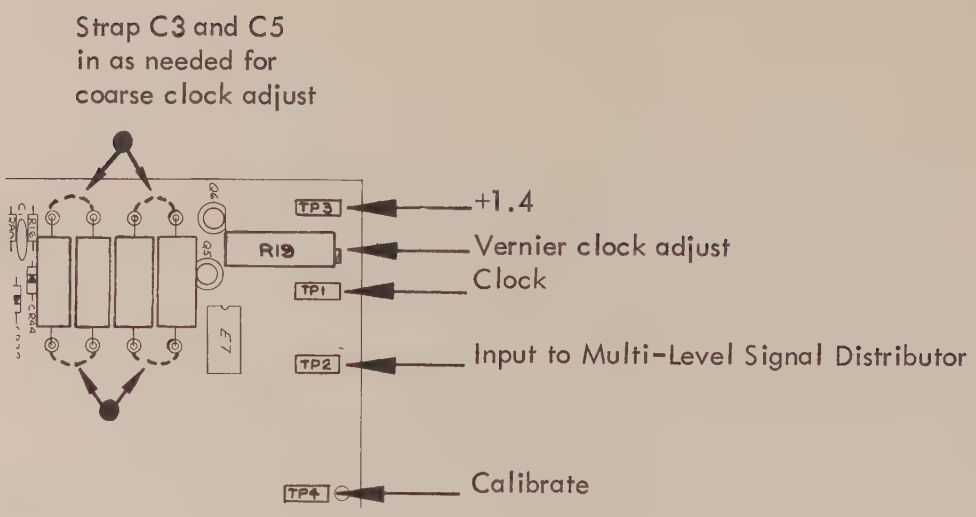


Figure 6-1

6.4 Test points are as follows:

Test Point (TP)	Color Coded	Shows
TP1	Red	Clock
TP2	Red	Input
TP3	Black	+1.4V reference
TP4	White	Calibrate

C3 and C5 are the course adjustment and R19 the vernier adjustment. See table below:

Baud	WPM	Capacitors
45.5	60	C2, C3 in parallel; C4, C5 in parallel
50	66	Same as 45.5 baud
56.8	75	C2; C4, C5 in parallel
74.2	100 (5 unit)	C2, C3 in parallel; C4
110	100 (8 unit)	C2; C4
150	200 (5 unit)	Change C2, C4 to .15 microfarads
180		Change C2, C4 to .12 microfarads
200		Same as 180 baud

If the desired speed can not be reached using one of the following calibration methods, it may be that the oscillator requires padding/trimming using C3 and/or C5.

a. Method 1: CALIBRATE CIRCUIT

(1) Equipment required.

(a) Voltmeter

(b) Signal source on the input loop that can generate a repeated character having at least one Mark-Space transition. For best accuracy, the character should have its next to last bit mark and last bit space; however, any character having a M-S transition can be used.

(2) Procedure:

(a) Place the voltmeter between TP4 and TP3. The positive (+) lead to TP4 and negative (-) lead to TP3. Voltage range should be +5V or higher.

(b) While the input loop is modulated by the repeated character, adjust the potentiometer for maximum deflection on the meter. Make sure that the character is printed properly on the printer, i.e. that the regenerated signal is the correct one.

b. Method 2: ELECTRONIC COUNTER

(1) Equipment required:

(a) An accurate ($\pm$0.1%) frequency/period counter.

(2) Procedure:

(a) Open the input loop to the selector. This allows the oscillator to free-run.

(b) Set both the START and STOP switches on the counter to measure from + to + (or - to -).

(c) Connect the reference lead to TP3. Connect the counter input lead to TP1.

(d) Adjust the potentiometer until the desired pulse width (1 bit) is obtained on the counter. See table below for typical pulse widths:

BAUD RATE	PULSE WIDTH IN MILLISEC
45.5	21.955
56.8	17.589
74.2	13.472
110	9.09

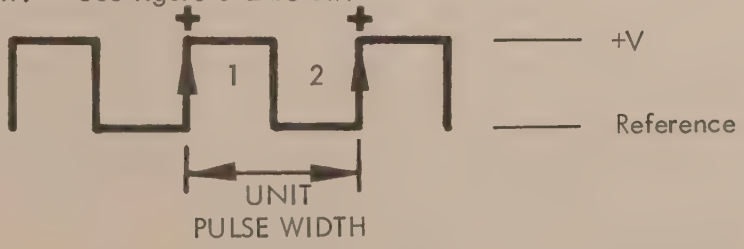
c. Method 3. OSCILLOSCOPE

(1) Procedure

(a) Follow the procedure outlined for Method 2 except that the pulse width is measured by observing the time between successive + to + (or - to -) transitions on the scope. Both pulses, 1 and 2, are equal in time duration. The time between the two positive going transitions should be equal to 1 bit. See figure 6-2 below:

Figure 6-2

Waveform at TP1:



7. CIRCUIT DESCRIPTION

7.1 Basic Block diagram:

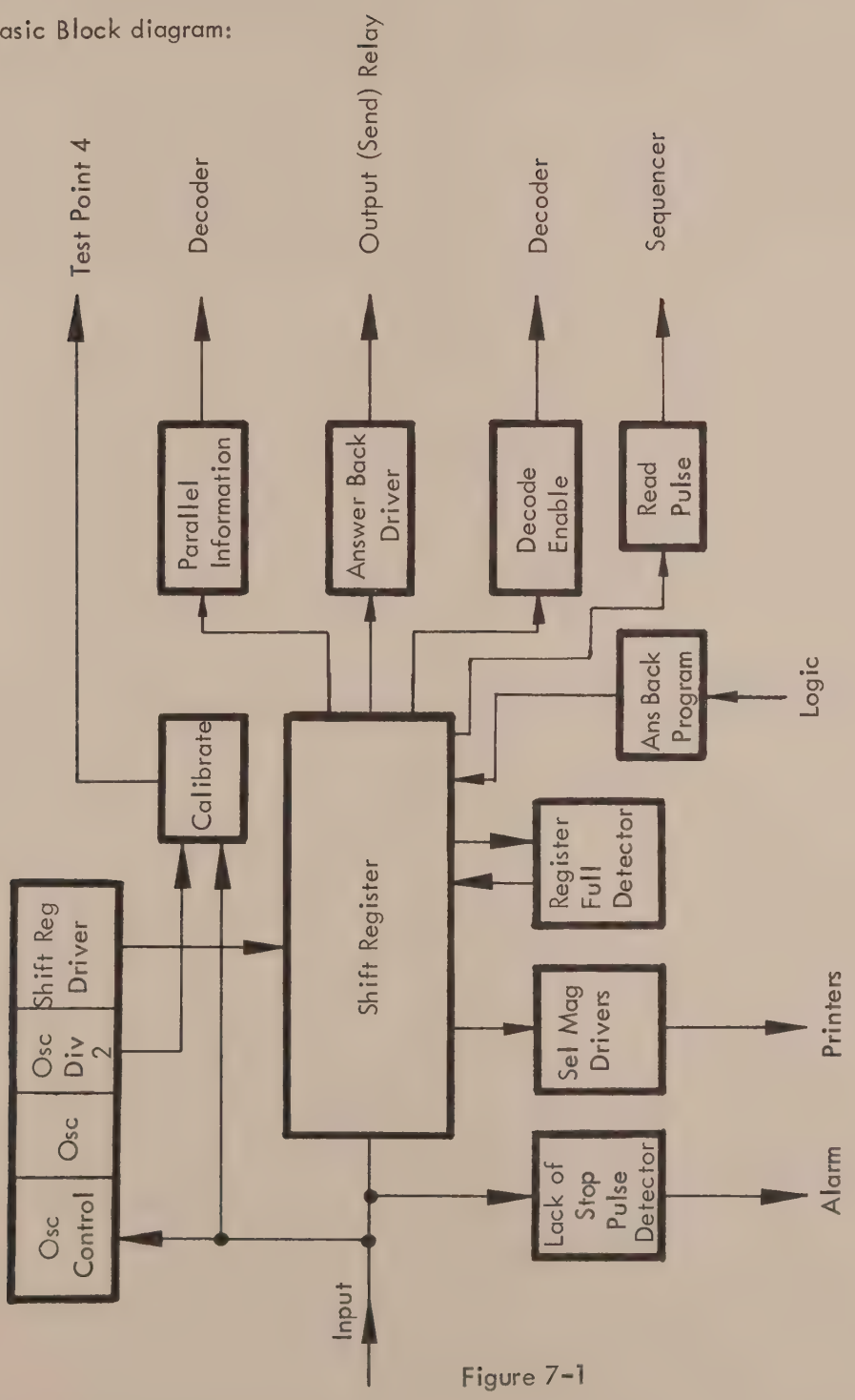


Figure 7-1

7.2 Refer to the schematic drawing, E200363.

7.3 The Multi-Level Signal Distributor has the following sections:

a. Shift register

b. Oscillator control circuit

c. Oscillator (multivibrator)

d. Oscillator divide by two (flip-flop)

e. Shift register driver (pulse amplifier)

f. Read Pulse generating circuit

g. Register full detection circuit

h. Lack of Stop Pulse Detection circuit

i. Two selector magnet driver circuits

j. Four answer back programming circuits (includes answer back Buffer flip-flop and answer back (send) relay driver circuit)

k. Calibrate circuit

7.4 Shift Register: Consists of ten flip-flops (f-f). They are the STOP, Bits 1 thru 8 and START. These labels refer to where the marks/spaces (in terms of highs and lows) are stored when the character is entered into the register. As you look at the schematic, the character is considered to be entered into the pins on the lower half of the f-f, e.g. these points are P/O E6-6 (means Part of IC E6 pin 6), P/O E5-5, P/O E5-9 etc. Bits 6, 7 and 8 may or may not be used depending on the code level of operation.

General: The function of the shift register is to accept the information fed to it in serial form and feed it to a decoder in parallel form at the prescribed time. An oscillator (Q5, Q6) is used as the time base for a given speed (baud) of operation. The oscillator feeds a f-f that divides the oscillator output by a factor of two. The f-f in turn drives a one stage pulse amplifier (Q7) that pulses the input common to all f-f's in the register. The oscillator is keyed on by the first M-S transition (start pulse) of a character and off during the stop pulse.

7.5 Oscillator Control Circuit: Consists of AND gate CR38, 39, 40, 41 and 42, transistor Q19 and Inverter (Inv.) P/O E9-5, -6. All inputs to the gate are Normally High (NH), Q19 Normally Low (NL) and E9-6 NH. If any one of the inputs goes low, Q19 goes high and E9-6 low enabling the oscillator. Inputs to the gate are:

a. Q5 collector at CR39 NH. This point follows the highs/lows at the collector of Q5

as the oscillator free-runs. The other inputs to the gate are arranged such that when a character has been entered into the shift register the other four leads are high and Q5 low; when Q5 goes high, all inputs to the gate are high; the result is Q19 goes low, E9-6 high turning off the oscillator.

b. Answer back control lead E8-12 at CR42 NH. When one of the answer back f-f's is activated, E8-12 goes low, Q19 high and E9-6 low enabling the oscillator. After the programmed character (answer back) has been shifted out of the register, the Register Full detection circuit output, E9-4, goes low (momentary) resetting the answer back flip-flop that set. On reset, E8-12 goes high, Q19 low, E9-6 high turning off the oscillator.

c. Loop input at CR41 NH. When the loop goes space (M-S) transition the input changes state and CR41 goes low, Q19 high, E9-6 low enabling the oscillator. This input follows the marks/spaces (in terms of highs/lows) on the external loop as seen by the Input Relay.

d. STOP bit, E6-6, at CR38, NH: This point follows the external loop variations at each clock pulse. The first clock pulse is generated 50% of a unit pulse after the M-S transition (start pulse).

e. START bit, E1-6, at CR40, NH: After the oscillator has been started by the start pulse the register is clocked 50% of a unit pulse later and the START bit f-f changes state and E1-6 goes low. This low enables the oscillator thru the last clock pulse. At the last clock pulse the START bit f-f is reset and E1-6 goes high. At this time the gate has only one low input at CR39, Q5's collector. On Q5 high the oscillator turns off as described in (a) above.

7.6 Oscillator: Consists of transistors Q5 NH, and Q6 NL. The oscillator is an astable multivibrator and is enabled when there is a low at E9-6. It has non-symmetrical waveform outputs.

7.7 Oscillator Divide by Two: Consists of IC E7. This f-f changes state everytime Q5 goes low. Its output at E7-6 NL, is a square wave. E7-9 NH is the test point (TP) 1 on the PC board.

7.8 Shift Register Driver (pulse amplifier): Consists of transistor Q7 NL. Each time E7-6 goes low Q7 goes high momentarily. The off time of Q7 depends on the RC time constant of R23 (5.6K) and C6 (0.01 microfarads). When C6 charges to the proper value Q7 goes low again clocking the shift register (all pins 1 of the IC's except the STOP bit which is pin 2).

7.9 Read Pulse Generating Circuit: Consists of Q8 NL, and Q9 NH and Q10 NL. On the last clock pulse E1-5 goes low causing Q8 high for approximately 75 to 100 microseconds (NL-H-L). This leading pulse in turn causes Q9 NH-L-H; this pulse causes Q10 NL-H-L which is the Read Pulse. Duration of the Read Pulse is approximately 30 microseconds. The total time delay from the time E1-5 goes low to the time the Read Pulse is generated is approximately 50 microseconds.

7.10 Register Full Detector: Consists of AND gate CR26, 27, 28, 29, 30, 31, 32, 33, 34 and 35, Inv. Q2, NAND gates P/O E8-1, -2 and P/O E9-3, -4. Inputs at CR26 thru 34 are NH, CR35 NL, Q2 NH, E8-2 NL and E9-4 NH. This circuit is used in answer back appli-

cations to detect when the register is "full". Full in the sense that all inputs to the AND gate are high. This says that the answer back character that was programmed has been shifted out on line (cleared the register) and it is ok to reset the register. Refer to paragraph 7.13a. for details.

7.11 Lack of Stop Pulse Detection Circuit: Q11 is NH. If the loop goes spacing and there is no mark generated on the loop before the end of the character, the gate controlling Q11 will go high and Q11 low. The control gate consists of CR55, CR56 and CR57. CR55 goes to E9-2 and is normally low with the loop marking and will go high anytime the loop goes spacing. CR56 goes to E6-9 and is normally low. When the loop goes spacing the oscillator starts and on the first clock pulse E6-9 goes high. If no further marks appear on line, this point remains high. CR57 goes to E1-6 which is normally high. On the first clock pulse it goes low. On the last clock pulse it goes high again. This says that a character has been entered into the shift register. If the loop has not gone marking, then CR55 and CR56 are high, instead of low, enabling Q11 low.

7.12 Selector Magnet Driver Circuits: Consists of two identical circuits. AND gate CR58, 59 and 60, Inv. E9-10, -11 and transistor Q12; AND gate CR61, 62, 63, Inv. E9-8, -9 and transistor Q3. Both operate in the same manner. Using Magnet Drive 2 as an example. Input at CR58 is NL, 59 and 60 NH, E9-10 NH and Q12 NL. CR59's input goes low only when a lack of stop pulse is detected and Q11 goes low. CR60's input goes low only when there is an answer back generated and E8-12 goes low. In both cases this low ensures Q12 low. CR59's low keeps the printer from running open and CR60's low keeps the printer from seeing the answer back. Anytime the STOP bit changes state (at a clock pulse if the input loop has changed state since the previous clock pulse) the input at CR58 changes state. For CR58 (loop gone space) E9-10 goes low causing Q12 high.

7.13 Answer Back Programming Circuits: There are four identical circuits for programming the shift register with an answer back character. They are Q13, 14, 15 and 16. All are NH. Q13 and Q14 are permanently connected. Q15 and Q16 are for programming the second answer back character. Q13 and 14 are controlled by an external source at pins 13 and 11 of the PC edge connector respectively. Both pins are NL. Q15 and 16 are also controlled by an external source at pins L and J respectively. Transistors Q17 and Q18 are used to activate the second answer back programmer thru straps at E and F. Additional circuitry used consists of two flip-flops, E8-3, -4, -5, -6 (NL, NH, NH, NL); E8-8, -9, -10, -11 (NL, NH, NH, NL); Inv. E9-12, -13 (NL, NH) and Inv. E8-12, -13 (NH, NL). Typical operation is as follows:

a. Pin 11 or 13 of the PC edge connector goes momentarily high. Assume 13. Q13 goes low. This low is applied thru CR72 to the STOP bit f-f pin 5 setting it, pin 6 low, 9 high. Also the low is applied to the group of diodes at point "A" (CR19 thru CR24) setting any bit that has its set lead connected to the anode of one of the diodes. This programs a space in that bit for the answer back character. The low is also applied thru CR73 setting the f-f, E8-8 high, E8-10 low. E8-10 low thru CR77 causes E9-12 high removing the clamp (low) from the Buffer f-f (thru CR37 to pin 10). At the same time, E8-12 goes low. This low is applied thru CR78 to inhibit the Read Pulse generating circuit. Also, the low is applied to CR60 and CR63 to keep the printer(s) in mark hold during the answer back, to CR42 to keep the oscillator on and to pin 11 of the STOP bit to inhibit the input to the register. The setting of the STOP bit (pin 5) is done so that this space shifts down the register keeping the register full gate from being acti-

vated until the programmed character clears the register. It is referred to as a "synthetic" start pulse. As the clock pulses are generated, the programmed information is fed thru the Buffer f-f to Q1 the answer back (send) driver. When the synthetic start pulse reaches the Buffer f-f, all bits to the register full gate are high (CR26 thru CR35) and Q2 goes low. This low does the following:

(1) Resets the Buffer f-f thru CR49 at E1-10

(2) Is fed to E8-1 and inverted to a high at E8-2 (cathode of CR50)

CR50 is ANDed with CR51. At the time CR50's input goes high the oscillator input to CR51 is low. When the input at CR51 goes high (Q5 high), E9-4 goes low (E1-4) resetting the START bit, pin 5 low, 6 high. Also this low resets the answer back control flip-flop thru CR75. E8-10 goes back high and -8 low. This removes the inhibits, from the input (E6-11), the selector magnet drive circuits (CR60 and 63) and the Read Pulse generating circuit (at CR78). On -8 low, Q18 is pulsed and goes high for a time determined by the RC time constant (R67) (C21), which is the STOP element time. When Q18 goes low it pulses Q17 high for a time determined by the RC time constant (R70) (C23). The pulse at Q17 is then used to initiate the second answer back character by enabling either Q15 or Q16 (provided strap E and/or F is/are made). Q15 or Q16 are in turn enabled as either/or by control leads at pins L and J respectively. Either high will allow the NL-H-L pulse at Q17 to cause the transistor selected momentarily low. This low is used to program the shift register in the same manner as did Q13. Q15 thru the diodes at C or Q16 at D. The associated control flip-flop is E8 pins -3, -4, -5 and -6. The sequence of events is again repeated as before. The control lead is returned low at some time T after Q17 has gone back low so that when it goes high again after the second character has been shifted out that it will not program another character.

7.14 Calibrate Circuit: Consists of Q4 (NL), Q20 (NL), Q22 (NH) and Q21 (NL). Q20 goes high at every M-S transition on the loop. The time Q20 remains high depends on the RC time constant (R30) (C8). Q4 goes high everytime pin 9 of the oscillator divide by two flip-flop goes low. The time Q4 remains high depends on the RC time constant (R33) (C11). If the oscillator is adjusted properly, at the instant the loop goes M-S, pin 9 of the oscillator divide by two is also going from high to low. These simultaneous H-L's cause Q22 to conduct momentarily pulsing Q21 on. Q21 on places battery (essentially) at the junction of R34, R35. The time for Q21 on depends on the time Q22 looks like a short which depends on the time constant (R32) (C9).

8. MAINTENANCE

8.1 Basic maintenance should be restricted to verifying that the built in oscillator is operating properly. Use the information in section 6. CALIBRATION.

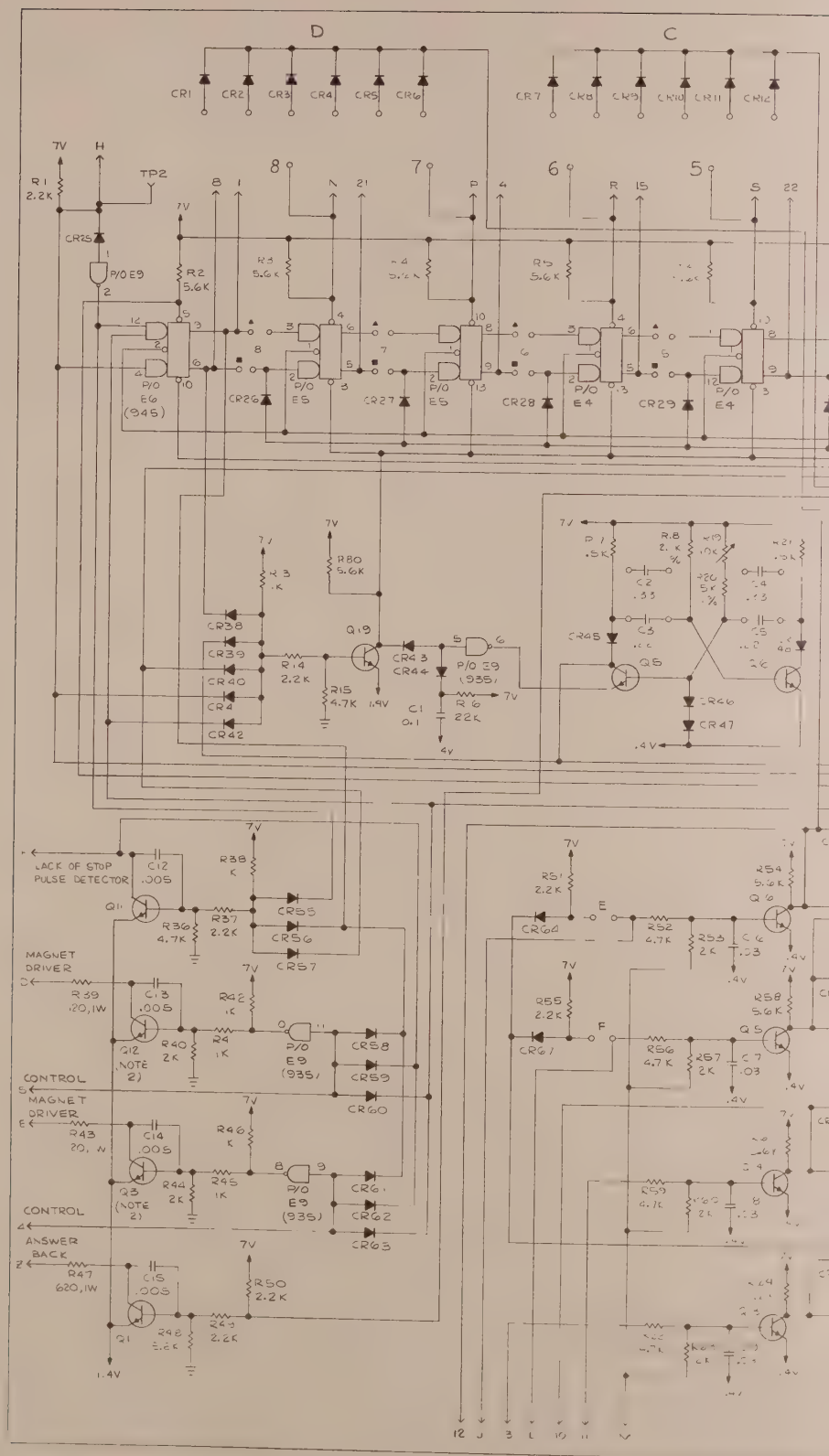
8.2 If troubles occur in a unit already in operation, substitution of PC boards that are correctly programmed and that are known to be in good working order should be tried first. The bad PC board(s) should be returned to the factory for repair. If there are no PC boards available and troubleshooting is the only alternative, refer to the information (SYMPTOM, POSSIBLE CAUSE) in paragraph 8.3. The information furnished assumes that the technician is familiar with logic diagrams, symbols, gates, etc. Before proceeding, it is suggested that the technician study APPENDIX I, Troubleshooting Pulsecom Selectors (last section in the selector manual) and section 7. CIRCUIT DESCRIPTION of the Sig XD instructions (preceding section).

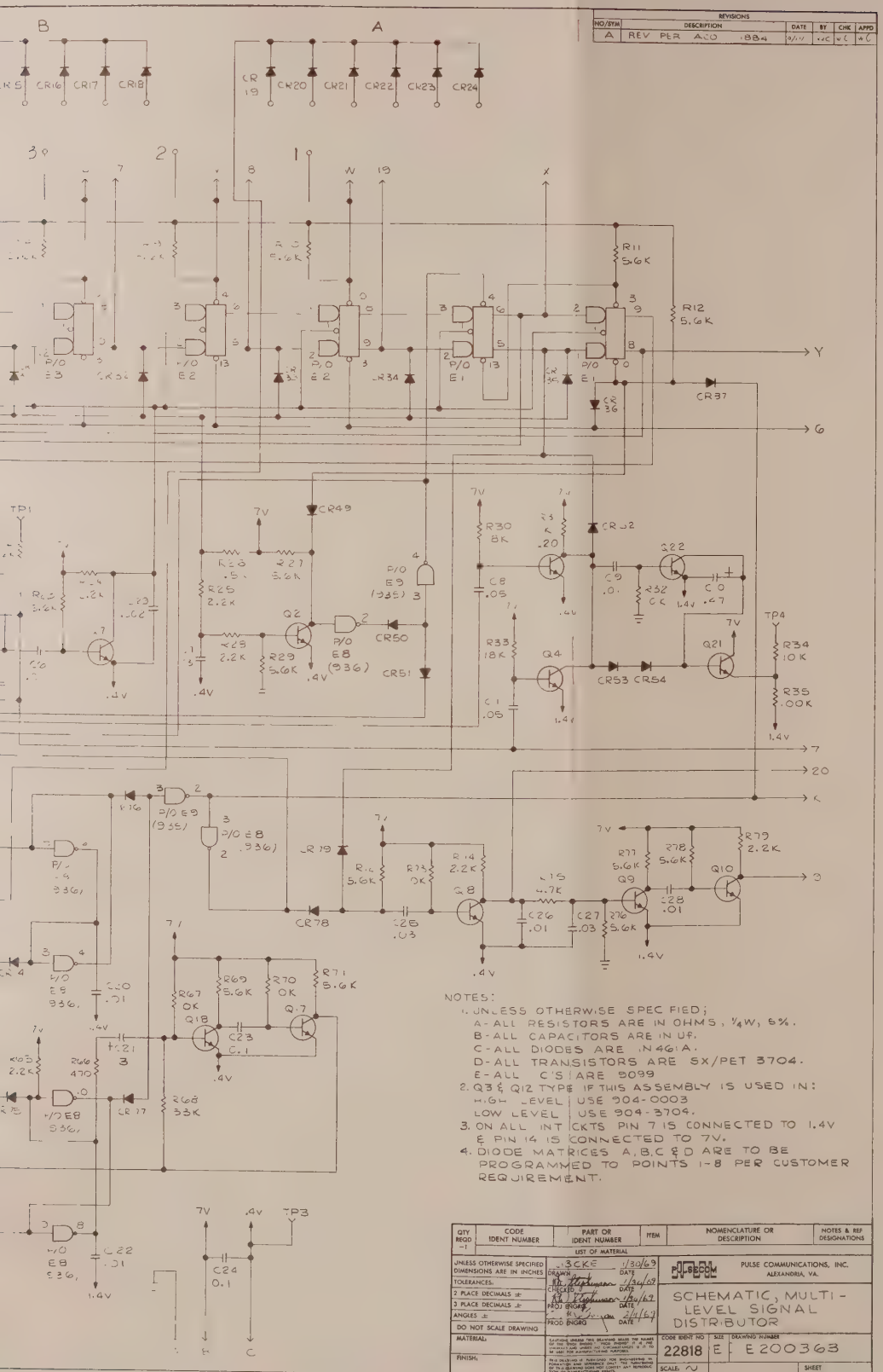
8.3 In order to troubleshoot the Sig XD properly, the technician will need an oscilloscope (oscilloscope should be capable of passing a 1MHz sine wave) and an "extension board" for extending the PC board out of the chassis for easy access to components, etc. Typical symptoms and their possible causes are listed below. If the components listed check out ok, then the associated circuitry should be carefully checked. These symptoms assume that basic troubleshooting procedures on the selector have already been performed, such as, checking line voltage, fuse, power supply, proper input signs, etc. Refer to the schematic drawing E200363 and the PC assembly drawing D501377.

SYMPTOM(S)	POSSIBLE CAUSE(S)
Pin H on PC edge connector does not go high/low as input loop varies	Input relay bad Incorrect biasing on input relay Incorrect wiring of input relay Incorrect loop current Open lead from PC edge connector to relay
Oscillator does not start when pin H goes low (M-S)	CR40 open Q19 bad CR43 bad P/O E9-5, -6 bad Q5 or Q6 bad
Oscillator runs continuously	One of the inputs to the oscillator control gate is locked low (CR38, 39, 40, 41, 42) Q19 bad CR43 bad (open)
Oscillator runs but divide by two does not	E7 bad

SYMPTOM(S)	POSSIBLE CAUSE(S)
Oscillator and E7 function but no clock pulses into register	Pulse amplifier bad (Q7) C6 bad Bad IC in shift register
Input signals do not feed into register	CR25 bad P/O E9-1, -2 bad E6-11 low (answer back f-f set) One of f-f's in register bad (including Buffer)
Answer back will not program into register	Answer back programmer(s) bad (Q13, Q14, Q15 or Q16) Diodes at "A", "B", "C" or "D" not programmed
Answer back programmes but will not shift out on line	Buffer f-f bad Q1 (answer back relay driver) bad Answer back relay bad Incorrect biasing on answer back relay
Answer back sent but system does not reset	Bad diode in register full detection gate (CR26 thru CR35) Q2 bad CR36, 37, 49, 22 bad E8-1, -2; E9-3, -4 bad
Read Pulse not generated	Q8, Q9 or Q10 bad CR79 bad
Selector magnet driver circuit(s) run open (space hold)	Q3, Q12 bad CR58, 59, 60, 61, 62, 63 bad STOP bit bad, pin 9 high
Selector magnet driver circuit(s) run closed (mark hold)	STOP bit bad, pin 9 low CR58, 59, 60, 61, 62, 63 bad One of answer back control f-f's set and inputs to CR60, 63 low Q3 or Q12 bad

SYMPTOM(S)	POSSIBLE CAUSE(S)
Lack of stop pulse detector gate functions but no alarm output at pin F	Q11 bad
Calibrate circuit does not function	Q4, 20, 22, 21 bad C8, C11, C9 bad CR53, 54 bad


D
C
CR1
CR2
CR3
CR4
CR5
CR6
CR7
CR8
CR9
CR10
CR11
CR12
7V
H
TP2
R1
2.2K
CR25
P/O E9
R2
5.6K
P/O E6 (945)
CR26
P/O E5
CR27
P/O E5
CR28
P/O E4
CR29
P/O E4
R80
5.6K
R3
1K
CR38
CR39
CR40
CR41
CR42
Q19
R14
2.2K
R15
4.7K
1.9V
CR43
CR44
P/O E9 (935)
R16
22K
C1
0.1
4V
R1
1.5K
R18
2.2K
1%
C2
.33
C3
C5
CR45
Q5
CR46
CR47
.4V
LACK OF STOP PULSE DETECTOR
C12
.005
Q11
R36
4.7K
R37
2.2K
R38
1K
CR55
CR56
CR57
MAGNET DRIVER
R39
120, 1W
C13
.005
Q12 (NOTE 2)
R40
2K
R42
1K
R41
1K
P/O E9 (935)
CR58
CR59
CR60
CONTROL
MAGNET DRIVER
R43
120, 1W
C14
.005
Q3 (NOTE 2)
R44
2K
R46
1K
R45
1K
CR61
CR62
CR63
CONTROL
ANSWER BACK
R47
620, 1W
C15
.005
Q1
R48
2.2K
R49
2.2K
R50
2.2K
1.4V
R51
2.2K
CR64
R52
4.7K
R53
2K
C6
.03
Q6
R54
5.6K
R55
2.2K
CR67
R56
4.7K
R57
2K
C7
.03
Q5
R58
5.6K
R59
4.7K
R60
2K
C8
.03
12
J
3
L
10
11
V



REVISIONS					
NO/SYM	DESCRIPTION	DATE	BY	CHK	APPD
A	REV PER ACO 1884	9/11	[illegible]	[illegible]	[illegible]

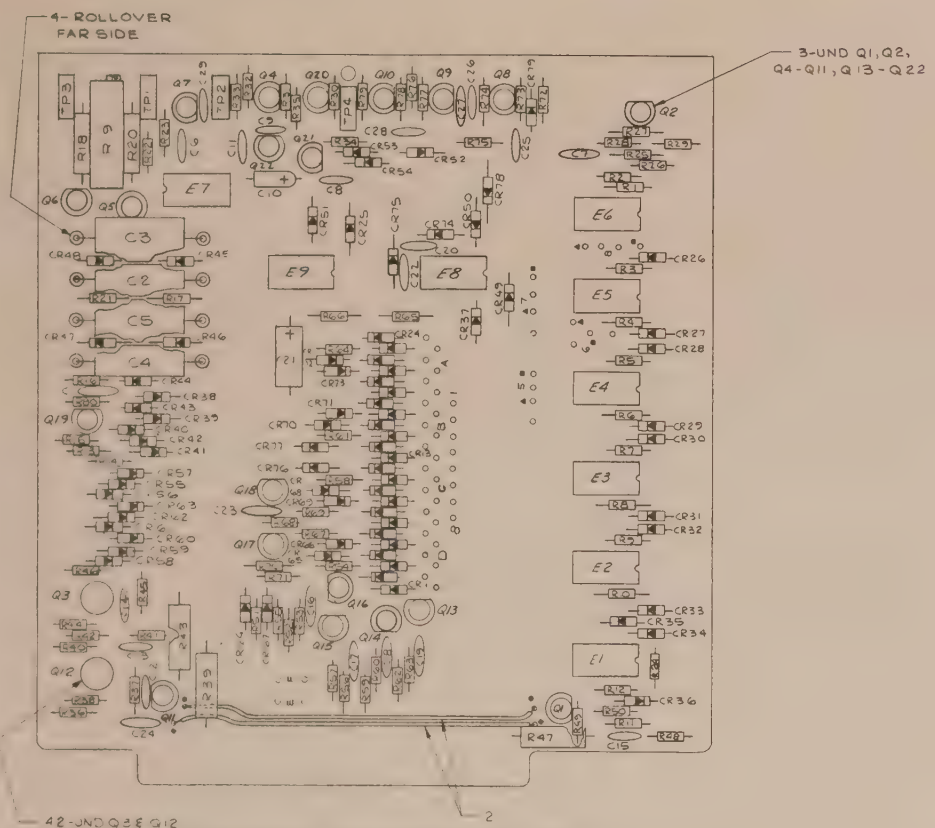
NOTES:

1. UNLESS OTHERWISE SPECIFIED;
   A - ALL RESISTORS ARE IN OHMS, 1/4W, 5%.
   B - ALL CAPACITORS ARE IN UF.
   C - ALL DIODES ARE 1N461A.
   D - ALL TRANSISTORS ARE SX/PET 3704.
   E - ALL C'S ARE 9099
2. Q3 & Q12 TYPE IF THIS ASSEMBLY IS USED IN:
   HIGH LEVEL | USE 904-0003
   LOW LEVEL | USE 904-3704.
3. ON ALL INT CKTS PIN 7 IS CONNECTED TO 1.4V & PIN 14 IS CONNECTED TO 7V.
4. DIODE MATRICES A, B, C & D ARE TO BE PROGRAMMED TO POINTS 1-8 PER CUSTOMER REQUIREMENT.

QTY REQD	CODE IDENT NUMBER	PART OR IDENT NUMBER	ITEM	NOMENCLATURE OR DESCRIPTION	NOTES & REF DESIGNATIONS
-1		LIST OF MATERIAL			

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DRAWN JCKE	1/30/69 DATE	PULSE COMMUNICATIONS, INC. ALEXANDRIA, VA.
TOLERANCES:	CHECKED [illegible]	2/4/69 DATE	
2 PLACE DECIMALS ±	APPROVED [illegible]	2/4/69 DATE	SCHEMATIC, MULTI-LEVEL SIGNAL DISTRIBUTOR
3 PLACE DECIMALS ±	PROJ ENGRG	DATE	
ANGLES ±	PROD ENGRG	DATE	
DO NOT SCALE DRAWING			
MATERIAL			CODE IDENT NO. 22818 | SIZE E | DRAWING NUMBER E200363
FINISH			SCALE: NONE | SHEET

REVISIONS				
NO/SYM	DESCRIPTION	DATE	BY	CHK	APPD



ITEM	REFERANCE DESIGNATIONS
4	Q1, Q2, Q4 THRU Q11, Q13 THRU Q21, Q22
20	R1, R14, R24, R25, R28, R37, R49, R50, R51, R55, R65, R74, R79.
21	R2 THRU R12, R22, R23, R27, R29, R48, R54, R58, R61, R64, R69 R71, R72, R76, R77, R78, R80.
22	R13, R31, R38, R41, R42, R45, R46.
23	R15, R36, R52, R56, R59, R62, R75.
27	R32, R34, R67, R70, R73.
29	R40, R44, R53, R57, R60, R63.
32	C6, C9, C20, C22, C26, C28
33	C7, C16 THRU C19, C25, C27.

NOTES:
1. EITHER 801-0461 OR B500034 MAY BE USED.
2. Q3 & Q12 TYPES IF USE IN:
   A. HIGH LEVEL, 904-0003 WITH 82-0001 PAD.
   B. LOW LEVEL, 904-3704 WITH 82-0002 PAD.
3. 6 DIODES ARE ASSOCIATED WITH EACH POINT (A,B,C & D) THESE DIODES WILL BE PROGRAMMED TO POINTS 1 THRU 8 PER CUSTOMER REQ.
4. SEE SCHEMATIC FOR STRAPPING INFORMATION.

QTY REQD	CODE IDENT NUMBER	PART OR IDENT NUMBER	ITEM	NOMENCLATURE OR DESCRIPTION	NOTES & REF DESIGNATIONS
1		3404-0202	43	CAPACITOR .002	C 29
2		NOTE 2	42	PAD, TRANSISTOR	
REF		E200363	41	SCHEMATIC	
2		3316-9332	40	CAPACITOR, .33UF	C3, C5
2		3316-9222	39	.22UF	C2, C4
1		3341-9301	38	3UF, 50V	C21
3		3403-9102	37	0.1UF	C1, C23, C24
4		3403-0502	36	.005UF	C12-C15
1		3568-9472	35	.47UF, 35V	C10
2		3403-9503	34	.05UF	C8, C11
7		3403-9303	33	.03UF	SEE TABLE
6		3403-9103	32	CAPACITOR, .01UF	SEE TABLE
1		204-3302	31	RESISTOR, 33K, 1/4W, 5%	R68
1		204-4700	30	470Ω	R66
6		204-1202	29	12K	SEE TABLE
1		204-1003	28	100K	R35
5		204-1002	27	10K	SEE TABLE
2		204-1802	26	18K	R30, R33
3		204-1501	25	1.5K	R17, R21, R26
1		204-2202	24	22K	R16
7		204-4701	23	4.7K	SEE TABLE
7		204-1001	22	1K	
27		204-5601	21	5.6K	
13		204-2201	20	2.2K, 1/2W, 5%	SEE TABLE
1		202-6200	19	620Ω, 1W, 5%	R47
2		202-1200	18	120Ω, 1W, 5%	R39, R43
1		753-1502	17	15K, 1/2W, 1%	R20
1		753-1212	16	12.1K, 1/2W, 1%	R18
1		742-1002	15	RESISTOR, VAR 10K	R19
20		904-3704	14	TRANSISTOR	SEE TABLE
2		NOTE 2	13	TRANSISTOR	Q3, Q12
79		NOTE 1	12	DIODE, IN461A	CR1-CR79
1		700-0935	11	INT CKT, 935	E9
1		700-0936	10	INT CKT, 936	E8
2		700-0945	9	INT CKT, 945	E6, E7
5		700-9099	8	INT CKT, 9099	E1-E5
1		3390-0007	7	JACK, TEST POINT (W)	TP4
1		3390-0008	6	JACK, TEST POINT (BLK)	TP3
2		3390-0001	5	JACK, TEST POINT (R)	TP1, TP2
8		610-0011	4	TERMINAL, ROLLOVER	
20		82-0002	3	PAD, TRANSISTOR	
AR		708-SERES	2	WIRE, ELEC	
1		D50-378	1	BOARD, PC	

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
2 PLACE DECIMALS ± ~
3 PLACE DECIMALS ± ~
ANGLES ± ~
DO NOT SCALE DRAWING
MATERIAL ~
FINISH ~

DRAWN BCKC 7/6/69
CHECKED 7-14-69
PROJ ENGRG DATE
PROD ENGRG DATE

CAUTION: UNLESS THIS DRAWING BEARS THE NAMES OF THE "PROJ ENGRG" AND "PROD ENGRG" IT IS UNLIKELY AND UNDER NO CIRCUMSTANCES IS IT TO BE USED FOR MANUFACTURING PURPOSES.

THIS DRAWING IS SUPPLIED IF A END ITEM AS INFORMATION AND REFERENCE ONLY. AS SUPPLIED ON THIS DRAWING, DOES NOT CONSTITUTE ANY APPROVAL FOR MANUFACTURING PURPOSES

PULSECOM
PULSE COMMUNICATIONS, INC.
ALEXANDRIA, VA.

BOARD, PC ASSY, MULTI-LEVEL SIGNAL DISTRIBUTOR

CODE IDENT NO 22818
SIZE D
DRAWING NUMBER D501377
SCALE 2/1
SHEET

INSTRUCTION MANUAL

Distortion Monitor
Model C100432
Issue 1

IN#187
(11/69)

CONTENTS

1. GENERAL

2. INSTALLATION

3. ADJUSTMENTS

4. CIRCUIT DESCRIPTION

C100432 Drawing

C200443 Drawing

INSTRUCTION MANUAL

MODEL C100432 DISTORTION MONITOR

1. GENERAL

The Model C100432 Distortion Monitor plug-in, etched circuit board is used to check incoming telegraph signals against a reference clock. If a preset threshold of distortion is reached, (strap selectable at 25 or 37-1/2%), a one-shot will fire to pulse an error relay. The relay has two form B contacts that are available for indicators, alarms, or other such use.

2. INSTALLATION

Before installing a Model C100432 Distortion Monitor as a replacement part, check the old board for the presence of straps at H and L. If straps are present on the old board, put them on the new board before installation. If there are no straps on the old board, be sure that the new board has no straps — remove them if they are present.

These straps set the distortion threshold at 37-1/2% or 25%. Refer to paragraph 3.2 for full details.

Another strap may be present going from E1/9 to 1.4 v. Copy this strap from the old board.

3. ADJUSTMENTS

3.1 There is an adjustment to set the Distortion Monitor Clock to run at the same speed as the signal distributor clock. This adjustment must be made with the distortion monitor plugged into the selector in which it will operate. To adjust the Distortion Monitor Clock, proceed as follows:

1. Connect a dc voltmeter across TP1 and TP2. Plus to TP2, minus to TP1. The maximum voltage will be 7 volts.

2. Feed continuous signals to the selector to cause the clocks to run.

3. With the clocks running, adjust potentiometer R4 for a maximum reading on the voltmeter. This reading will be acout 4 volts. The level is not important. The important thing is to PEAK THE ADJUSTMENT FOR MAXIMUM INDICATION ON THE METER.

3.2 The threshold of distortion detection may be set to either 25% or 37-1/2%. To set the threshold of distortion detection at 25%, proceed as follows:

1. Remove the two jumpers marked H and L.

2. Perform the adjustment procedure outlined in paragraph 3.1.

To set the threshold of distortion detection at 37-1/2%, proceed as follows:

1. Add the two jumpers marked H and L.

2. Perform the adjustment procedure outlined in paragraph 3.1.

4. CIRCUIT DESCRIPTION

The circuits of the Model C100432 are divided into three parts (refer to Drawing C200443). First, transistors Q1 and Q2 are connected to form a multivibrator that is used as a timing reference Second, flip-flops E2 are combined with E3/6, E3/12, and E1/12 to form a comparator circuit for error detection. Third, transistors Q3 and Q4 along with E1/10 are connected to form a one-shot relay driver for signaling an error detection.

With no signals on the line, the distortion monitor will be held in a reset condition by a low on input pin 9. This low will place a high on the emitter of transistor Q1, holding the multivibrator off. This high at E1/6 will set a low at E1/4 to hold both flip-flops reset. Figure 4-1 illustrates the relationship in time between the various key signals. The reset condition is shown just prior to time 1.

Action begins with the first mark-to-space transition on the telegraph circuit. This beginning of a character's start element will have immediate effect on the distortion monitor. When this transition takes place, the run gate on pin 9 will go high. This removes the inhibit from the multivibrator, and removes the reset from the flip-flops. The resulting shift from high to low at the collector of Q1 will toggle the first flip-flop and then E2/6 will toggle the second flip-flop. The flip-flops will then continue to run as a two-stage binary counter.

The count from the flip-flops is used to gate circuits E3/6 and E3/12, the error gates. If the output of either of these circuits is low when a signal transition from mark-to-space, or space-to-mark occurs, an error will be signaled. Because the clock runs at four times the baud, eight time divisions are available, each one being 12-1/2% of the total. As shown, gate E3/6 becomes active from 25% into the cycle to 50% into the cycle and gate E3/12 becomes active from 50% to 75% of the cycle. This provides an error gate for signals distorted ±25%.

An error is signaled by passing current through either diode CR7 or CR8. The bias on these diodes is controlled by the error gates. If both gates (E3/6 and E3/12) are high, the diodes will be reverse biased through R16 and R17 and R7. But, when either gate goes low, diode CR7 will conduct through R16 and R10, while diode CR8 conducts through R17 and R10. Notice that capacitors C6 and C7 are connected to the cathodes of CR7 and CR8, respectively. The level

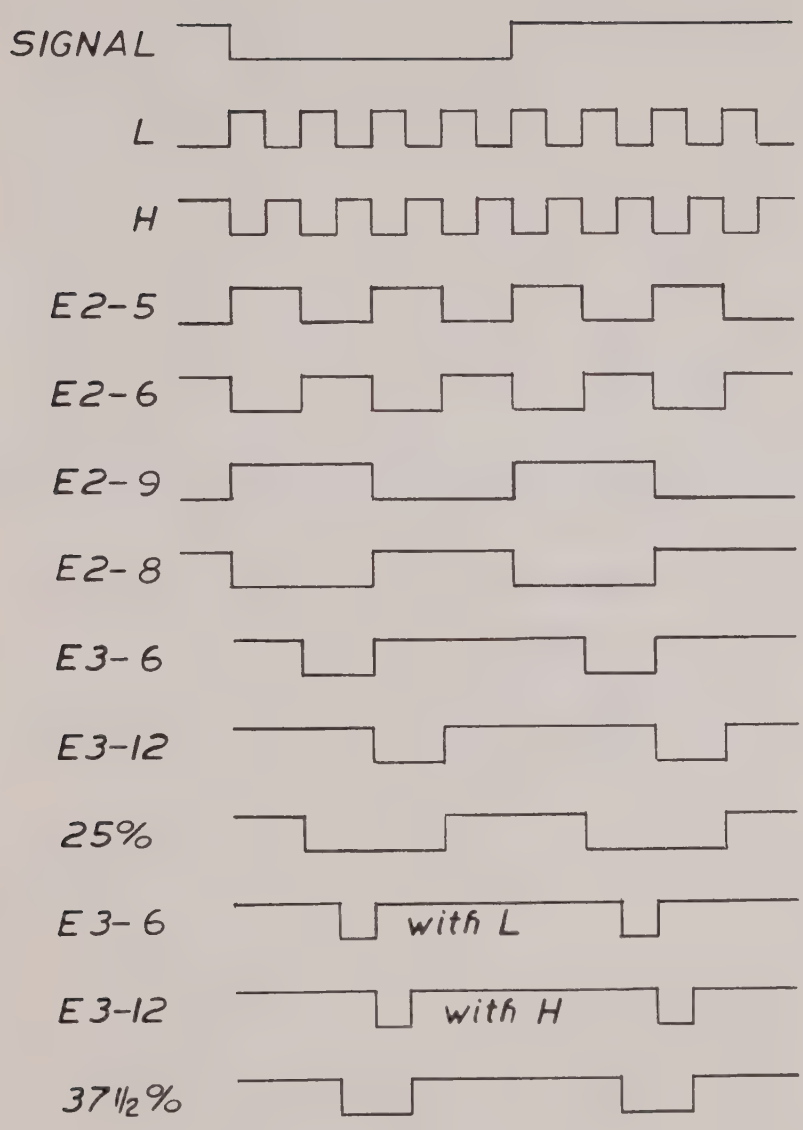


Figure 4-1. Timing Chart

established at the base of Q4 by the gate being open is such that a negative shift through either of these capacitors will cut Q4 off. Notice also that the signal applied to C7 is inverted and applied to C6. This signal at pin 12 is the data. Therefore, any transition on the loop during gate time will cause Q4 to cut off. The resulting high at the collector of Q4 will set a low at E1/10, charging C8. Capacitor C8 is tied back to the collector of Q4 to form a one-shot. Even though the pulse to turn Q4 off is short, it will remain off until C8 discharges. The resulting lengthened positive pulse at the collector of Q4 is used to turn Q3 on, the relay driver. Pin 11 is connected to the source for relay power, usually +24 volts.

When the relay operates, the normally open contacts on F and D, and 4 and C, are closed.

Input 10 is used to inhibit the error gate as desired. If this input is not to be used, E1/9 is tied to +1.4 v through a strap.

Jumpers H and L are made to change the error threshold from 25% to 37-1/2%. Connecting these straps adds conditions to E3/6 and E3/12 to restrict the gate to the phase of the multivibrator. Refer to the timing diagram.

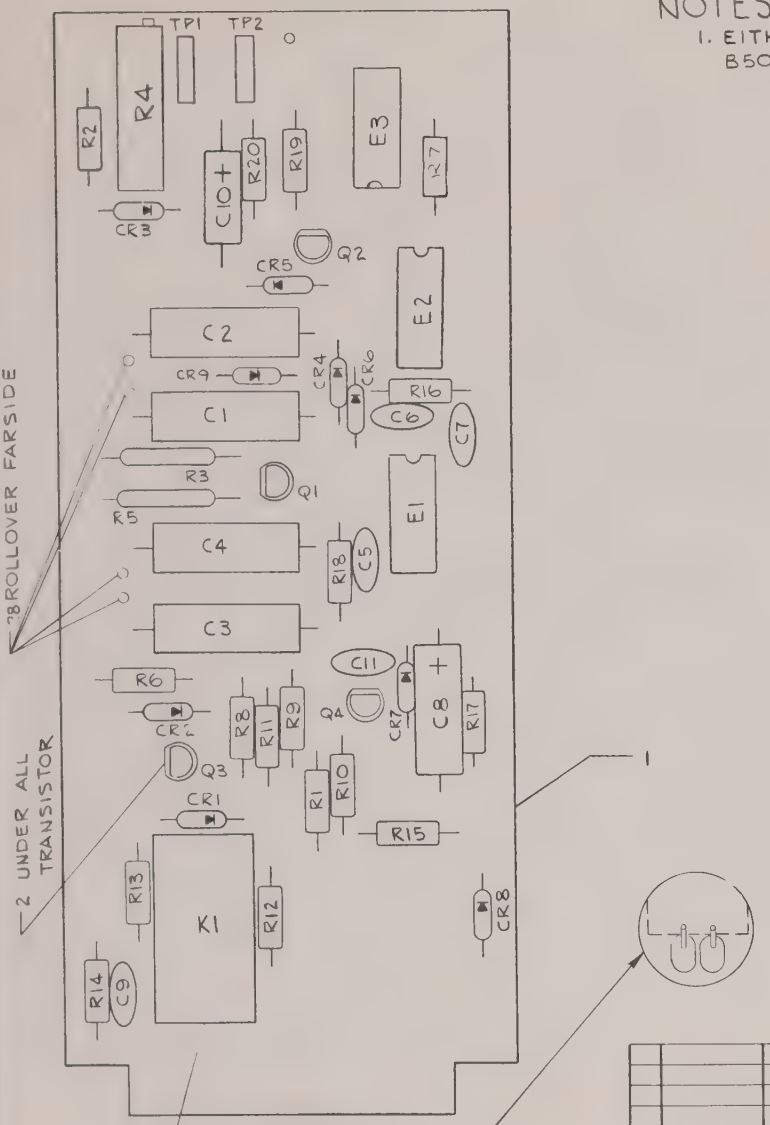
In summary, a distortion error is detected as follows:

1. Data starts the clock
2. The clock runs the flip-flop counter
3. The counter gates the errors
4. Errors trigger the one-shot
5. The one-shot activates the relay.

REVISIONS					
NO/SYM	DESCRIPTION	DATE	BY	CHK	APPD

NOTES:

1. EITHER 801-0461 OR B500034 MAY BE USED.



QTY REQD	CODE IDENT NUMBER	PART OR IDENT NUMBER	ITEM	NOMENCLATURE OR DESCRIPTION	NOTES & REF DESIGNATIONS
1		201-4709	31	RESISTOR 47Ω 1/2W 5%	R18
2		201-4708	30	RESISTOR 4.7Ω 1/2W 5%	R12, R13
1		3834-0015	29	RELAY, REED	K1
4		610-0011	28	TERMINAL ROLLOVER	
REF		C200443	27	SCHEMATIC	
1		3390-0001	26	TEST POINT RED	TP2
1		3390-0007	25	TEST POINT WHT	TP1
1		742-1002	24	RESISTOR VAR 10K	R4
1		201-4700	23	RESISTOR 470Ω 1/2W 5%	R19
3		201-5601	22	5.6K 1/2W 5%	R16, R17, R20
1		201-2008	21	2Ω 1/2W 5%	R14
1		201-4701	20	4.7K 1/2W 5%	R11
1		201-1502	19	15K 1/2W 5%	R10
1		201-2201	18	2.2K 1/2W 5%	R9
1		753-1212	17	12.1K 1/2W 1%	R5
1		753-7501	16	7.5K 1/2W 1%	R3
4		201-1001	15	1K 1/2W 5%	R2, R6, R7, R15
2		201-1501	14	RESISTOR 1.5K 1/2W 5%	R1, R8
9		SEE NOTE 1	13	DIODE IN461A	CR1 THRU CR9
1		3340-0100	12	CAPACITOR 10μf@25V	C10
1		3315-9102	11	.1 μf@10V	C9
1		3336-0101	10	100μf@6V	C8
2		3403-9103	9	.01 μf	C6, C7
2		3313-9303	8	.03 μf	C5, C11
4		3317-9152	7	CAPACITOR .15 μf	C1 THRU C4
1		700-0962	6	INT, CIRCUIT	E3
1		700-9093	5	INT, CIRCUIT	E2
1		700-0936	4	INT, CIRCUIT	E1
4		900-5449	3	TRANSISTOR 2N 5449	Q1 THRU Q4
4		82-0002	2	PAD, TRANSISTOR	Q1 THRU Q4
1		C501584	1	BOARD, PC	

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TOLERANCES:

2 PLACE DECIMALS ± ~

3 PLACE DECIMALS ± ~

ANGLES ± ~

DO NOT SCALE DRAWING

MATERIAL:

FINISH:

	DATE
DRAWN: Dungan J M	8-8-69
CHECKED: W. GLEADALL	8 AUG '69
PROJ ENGRG:	DATE
PROD ENGRG:	DATE

CAUTION: UNLESS THIS DRAWING BEARS THE NAMES OF THE PROJ ENGRG. "PROD ENGRG IT IS PRELIMINARY AND UNDER NO CIRCUMSTANCES IS IT TO BE USED FOR MANUFACTURING PURPOSES

THIS DRAWING IS FURNISHED FOR ENGINEERING INFORMATION AND REFERENCE ONLY. THE FURNISHING OF THIS DRAWING DOES NOT CONVEY ANY REPRODUCTION OR MANUFACTURING RIGHTS.

PULSECOM

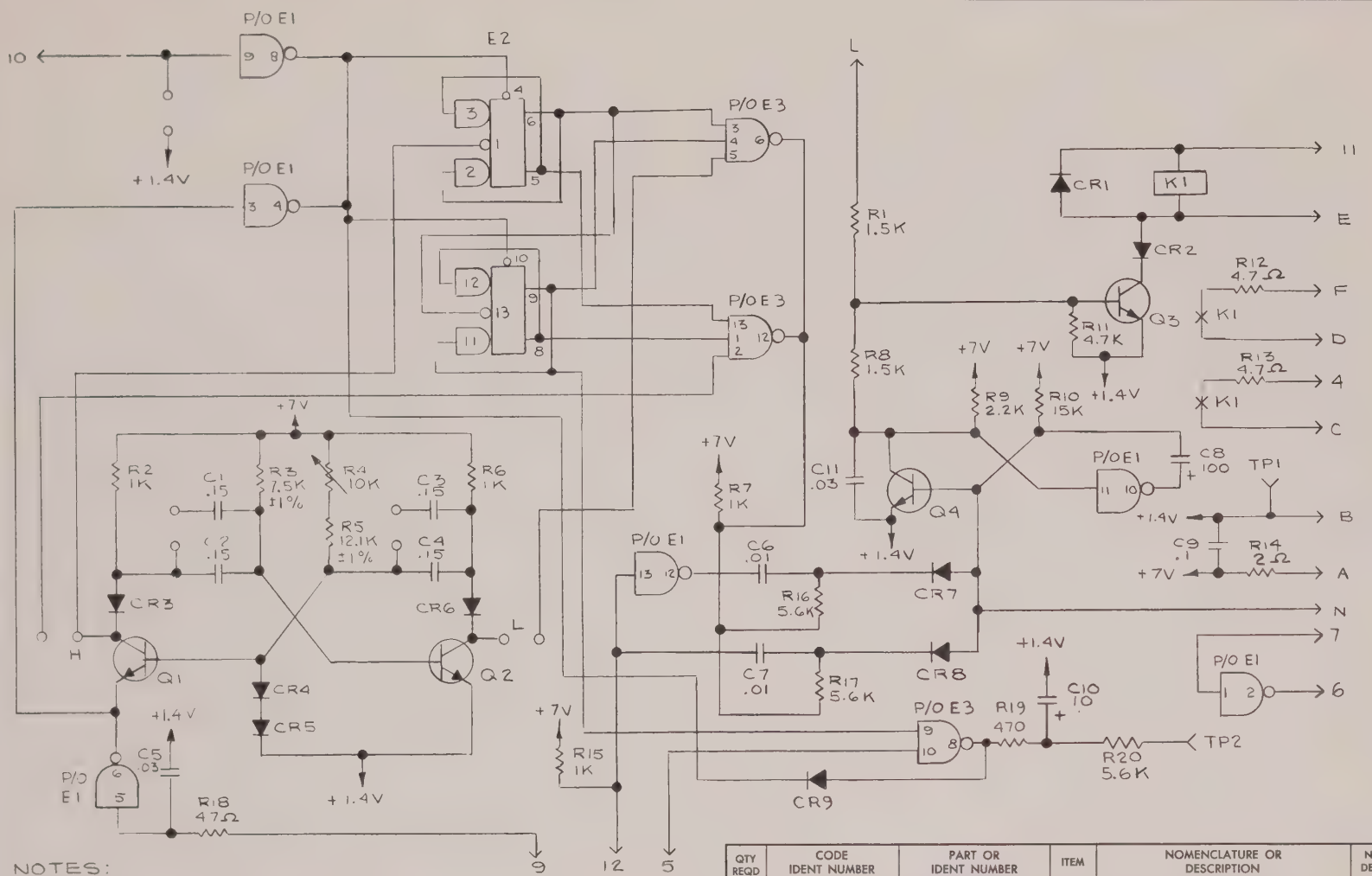
PULSE COMMUNICATIONS, INC.
ALEXANDRIA, VA.

BOARD P.C. ASSY DISTORTION MONITOR

CODE IDENT NO.	SIZE	DRAWING NUMBER
22818	C	C100432

SCALE: 2/1 SHEET

DASH NO.	NEXT ASSY	USED ON
	APPLICATION	



REVISIONS					
NO/SYM	DESCRIPTION	DATE	BY	CHK	APPD

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   - A- ALL RESISTORS ARE IN OHMS, 1/2 W, 5%.
   - B- ALL CAPACITORS ARE IN μf.
   - C- ALL DIODES ARE 1N461A
   - D- ALL TRANSISTORS ARE 2N5449
   - E- INT CKTS ARE AS FOLLOWS:
     E1: 936, E2: 9093, E3: 962

QTY REQD -1	CODE IDENT NUMBER	PART OR IDENT NUMBER	ITEM	NOMENCLATURE OR DESCRIPTION	NOTES & REF DESIGNATIONS

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DRAWN	7-31-69 DATE	PULSECOM PULSE COMMUNICATIONS, INC. ALEXANDRIA, VA.
TOLERANCES:	CHECKED	8/18/69 DATE	SCHEMATIC
2 PLACE DECIMALS ±	PROJ ENGRG	10/13/69 DATE	DISTORTION MONITOR
3 PLACE DECIMALS ±	PROD ENGRG	10/13/69 DATE	
ANGLES ±			
DO NOT SCALE DRAWING			
MATERIAL:	CAUTION: UNLESS THIS DRAWING BEARS THE NAMES OF THE "PROJ ENGRG." "PROD ENGRG" IT IS PRELIMINARY AND UNDER NO CIRCUMSTANCES IS IT TO BE USED FOR MANUFACTURING PURPOSES		CODE IDENT NO. 22818 / SIZE C / DRAWING NUMBER C200443
FINISH:	THIS DRAWING IS FURNISHED FOR ENGINEERING INFORMATION AND REFERENCE ONLY THE FURNISHING OF THIS DRAWING DOES NOT CONVEY ANY REPRODUCTION OR MANUFACTURING RIGHTS		SCALE: / SHEET /

DASH NO	NEXT ASSY	USED ON
	C100432	DSTN MON
	APPLICATION	

INSTRUCTION MANUAL

Power Supply
Model D500711
Issue 2

IN#144
(12/69)

ADDENDUM 1
(3/70)

INSTRUCTION MANUAL

Power Supply
Model D500711
IN#144
(12/69)

1. GENERAL

This addendum provides information on the Model D500711-7 Power Supply. For circuit description reference is made to applicable text and illustrations in the basic instruction manual.

2. SPECIFICATIONS

The Model D500711-7 Power Supply printed circuit board provides the following outputs:

+24 Volts, Unregulated
+ 7 Volts, Regulated
+2.1 Volts (reference)
+1.4 Volts (reference)

3. CIRCUIT DESCRIPTION

Refer to Schematic Diagram, Drawing C200527 and the basic manual.

+24 Volts, Unregulated.	A full-wave, filtered power supply. Provides base current for Q4 thereby increasing the current capacity of the +7 volt regulated supply.
+7 Volts, Regulated.	Refer to paragraph 4.4 and Figure 4 of the basic manual.
+2.1 and +1.4 Volts (reference).	Refer to paragraph 4.6 of the basic manual.

4. DRAWINGS

D500711, Rev. R — Board P.C. Assy, Power Supply, Sheet 1 of 3
D500711, Rev. M — Board P.C. Assy, Power Supply, Sheet 2 of 3
D500711, — Board P.C. Assy, Power Supply, Sheet 3 of 3
C200527, Schematic, Power Supply (7V and 1.4V)

IN#144
(12/69)

INSTRUCTION MANUAL

Power Supply
Model D500711
Issue 2

TABLE OF CONTENTS

	Page
1. GENERAL	1
2. MAINTENANCE	1
3. FACTORY SERVICE/SPARE PARTS	3
4. CIRCUIT DESCRIPTION	3
5. DRAWINGS	7

POWER SUPPLY BOARD

Model D500711

1. GENERAL

The Model D500711 Power Supply Board is a PULSECOM standard printed circuit assembly. It has been designed to supply up to three regulated dc output voltages, and two reference voltages. A dash-number suffix on the basic model number identifies the output of the board. For example: The Model D500711-1 supplies +7, +24, and +60 volts regulated plus a +1.4 and a +2.1V reference. The following table describes the outputs for the various dash numbers:

Dash Number	+60V	+24V	+7V	+5V	+1.4V & +2.1V	Schematic Number
1	X	X	X		X	C200188
2		X	X		X	C200210
3		X		X		C200349
4	X					B200409
5				X		C200476
6		X		X		C200505

2. MAINTENANCE

2.1 General

If a power supply failure should occur, the following procedure will help to isolate the trouble. Normally, the only test equipment required will be a volt-ohm meter.

In the case of power supplies, circuit substitution may not determine if the trouble is in the supply or not. This is because a failure external to the supply can damage the supply, or make it appear to fail. Therefore, the following procedure does not use circuit substitution. Begin with power removed, the power cord disconnected and if practical with all other printed circuits unplugged.

(1) Does the failure cause the input fuse to blow? If it does, go to step 2. If it does not, go to step 5.

(2) Unplug the power supply board.

(3) Using an ohm-meter, check the resistance between the outputs and common. Although the resistance may be low, no direct short to ground should exist. If a short to ground does exist, the trouble is not in the supply and will be found elsewhere. When a fault of this type occurs, the supply may be damaged. If the supply does not function properly after removing the short, proceed with the next step.

(4) Check the front-to-back and back-to-front resistance of CR1, CR2, CR3, CR4, and CR5 for an open or short.

(5) Replace the power supply board and apply power. Using the voltmeter, check for the following readings. Note: the following voltages are nominal and given only as a guide. Component variations within their normal tolerances will cause some variation. However, gross variations should not occur. All readings are with respect to ground.

Check the cathode of the reference Zener diodes:

CR7 Type 1N759A, 12 volts
CR8 Type 1N750A, 4.7 volts
CR8 Type 1N748A, 3.9 volts

(6) Check the voltage on the positive terminal of C1 for 100 volts nominal, C3 for 50 volts nominal, C5 for 16 volts nominal, and C6 for 16 volts nominal. These are the unregulated voltages for the +60, +24, +7, and +5 volt supplies. Their values will vary widely with load and input voltage.

(7) During normal operation, all transistors will be forward biased and conducting. Therefore, the bases of Q1 through Q5 and the chassis mounted regulator transistors will be nominally 0.6 volt above their emitters. Diode CR12 will also be in continuous conduction; thus the voltage dropped across CR12 should be 0.6 volt.

2.2 Maintenance and Repairs

There are no routine maintenance procedures required for the Type D500711 Power Supply Board. However, if repairs are made, certain procedures should be used to accomplish the repairs, and after any component has been replaced the output voltages should be checked for proper level.

When replacing a component part, care should be used to prevent overheating the board or the component. Use only enough heat to make a good solder joint. Also, when placing the component on the board, make a strain relief loop to avoid component damage. This is especially important for glass diodes.

After making the repair, check the output voltages. The output voltages should be +60 ±2 volts, +24 ±1 volt, +7 ±0.5 volt, +5 ±0.5 volt. If they are not within tolerance, a resistor will need to be changed. Before doing this, be certain that no circuit component is defective and that the supply is not overloaded.

If the +60 volt supply requires adjustment, remove R7 and connect a decade resistance box in its place. Adjust the decade box to obtain an output within tolerance. Note the resistance value indicated. Remove the decade box and install a resistor of the value indicated, or as close to that value as possible while maintaining output tolerance. The same procedure applies to the +24 volt supply, except R11 is substituted. The +7 volt and +5 volt supplies are adjusted by substituting for R16. In all cases, increasing the value of the resistor will increase the output voltage.

3. FACTORY SERVICE/SPARE PARTS

3.1 Factory Service

Promp service can be obtained by returning the defective unit, transportation prepaid to the factory. When the unit is shipped, the plug-in printed circuit boards should be removed and wrapped separately.

Include a purchase order describing the nature of the defect and the repairs authorized.

3.2 Spare Parts

When ordering spare parts or assemblies, describe by Model and Serial number the equipment in which the spare parts or assemblies are to be used. Order all parts and assemblies by Pulsecom part number.

3.3 Ordering Information

Send orders for both parts and service to:

Pulse Communications, Inc.
5714 Columbia Pike
Falls Church, Virginia 22041

Telephone: 703/481-0652
Telex: 89-9423

4. CIRCUIT DESCRIPTION

4.1 +60V Power Supply (Refer to Figure 1)

Figure 1 is a schematic diagram that shows the components used by the +60V supply, including the external regulator transistor. This latter component is mounted on a heat sink external to the printed circuit board.

The ac power from the power supply transformer secondary is half-wave rectified by CR1 and filtered by C1. The resulting unregulated dc power is supplied to the collector of the regulator, and to the control circuits of the regulator. This voltage is applied to the base

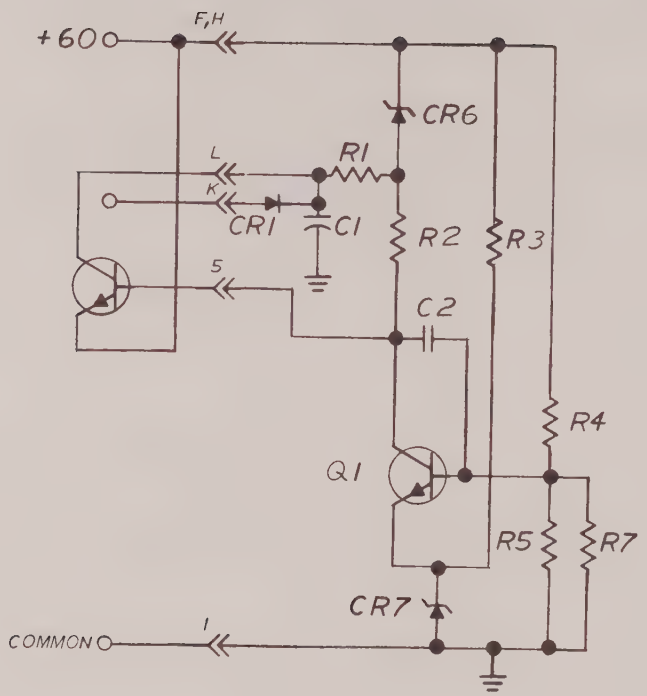


FIGURE 1

of the regulator through R1 and R2. Because the base is now more positive than the emitter, the transistor will conduct and the output voltage will begin to rise. The regulator is an emitter follower. By maintaining control over its base voltage, the output voltage can be regulated. Transistor Q1 serves this purpose.

When the output voltage at pins F and H exceeds approximately 12 volts, Zener diode CR7 will conduct to establish a reference voltage at the emitter of Q1. Voltage divider R4-R5 provides a sample of the output voltage to the base of Q1. If the output voltage increases, the current through R4 and R5 will increase. This raises the base voltage at Q1, increasing its conduction and increasing the voltage drop across R2. In turn, the voltage at the base of the regulator is lowered, decreasing its conduction and returning the output voltage to its nominal value.

Zener regulator CR6 will conduct with 4.7 volts of reverse bias applied. The resulting reference between emitter and base limits the base current through the regulator, preventing a heavy start-up surge. Also, should a short circuit occur on the output, the current would be limited, preventing power supply damage until the fuse blows.

To compensate for differences in component value, resistor R7 is factory selected to adjust the output voltage as required.

4.2 +24 Volt Supply, D500711-1 (Refer to Figure 2)

Figure 2 is the schematic diagram showing the components used by the +24V supply. The incoming ac power for the +24 volt supply is full-wave rectified by CR2 and CR3, then filtered by C3. The resulting unregulated dc power is supplied to the collector of the regulator and to the regulator control circuit. Transistor Q3 is an error detection amplifier. Zener diode CR7 establishes a reference level at the emitter of Q3. A sample of the output voltage is applied to the base of Q3 from voltage divider R8-R9. As the load on the power supply changes, the output voltage tends to change. Any change in output current causes a current change through divider R8-R9, resulting in a change in the voltage at the base of Q3. For example: If the voltage decreases, the voltage at the base of Q3 decreases and therefore the current through Q3 also decreases. Note that the collector current of Q3 flows through R6. The voltage drop across this resistor is applied to the base of Q2. Because of decreased current flow through R6 the base of Q2 will go positive. This increases the current through Q2, raising the emitter voltage and thus the voltage at the base of the regulator. Because the voltage at the base of the regulator is increased, the current flowing through the regulator will increase. This increased current flow results in restoration of the voltage to +24 volts while furnishing the increased current demanded by the load.

Electrolytic capacitor C5 provides filtering of the output voltage. To prevent oscillation due to sudden load changes or stray feed-back, capacitor C4 provides degenerative feed-back in the error amplifier, Q3.

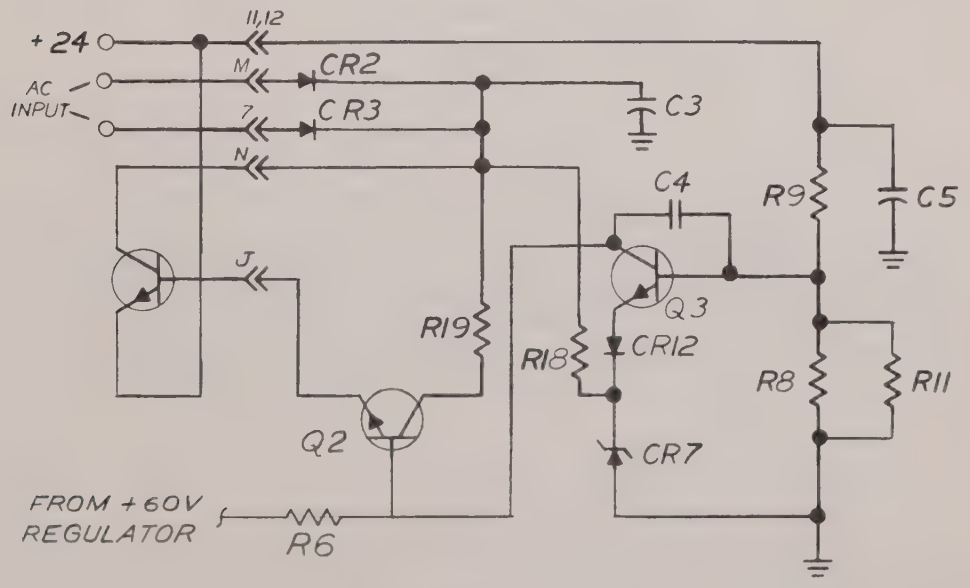


FIGURE 2

4.3 +24 Volt Supply (Refer to Figure 3)

Figure 3 is the schematic diagram of the +24V supply configuration when it does not share the PC board with a +60V supply. Operation of this supply is the same as the +24V supply described in paragraph 4.2 with a minor difference. The bias voltage for the base of Q2 is provided by R17 instead of through R6 from the +60V supply.

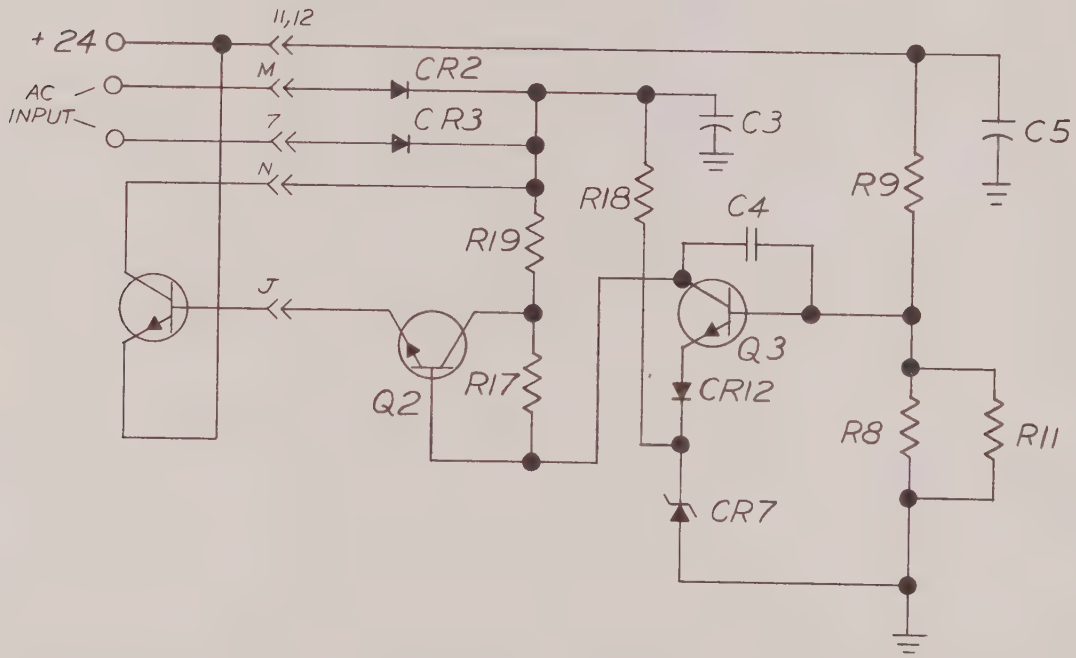


FIGURE 3

4.4 +7 Volt Supply (Refer to Figure 4)

The +7 volt supply functions in a manner almost identical to the +24 volt supply described in paragraph 4.3. Note that Zener diode CR8 furnishes the reference for the +7 volt supply. Transistor Q5 is the error amplifier. It compares the reference voltage provided by the Zener diode with a sample of the regulated output. The sample is taken at the junction of divider R13-R14. Transistor Q4 drives the base of the regulator. Its counterpart in the +24 volt supply is Q2.

4.5 +5 Volt Supply (Refer to Figure 4)

The +5 volt supply is substituted for the +7 volt supply. The value of reference diode CR8 is changed from a 4.7 volt Zener diode to a 3.9 volt Zener diode. Also, resistor R14 is changed from 1.5K to 5.6K to provide the proper output-voltage sample to the base of error amplifier Q5. Functionally, this circuit is identical to the +24 volt supply described in paragraph 4.3.

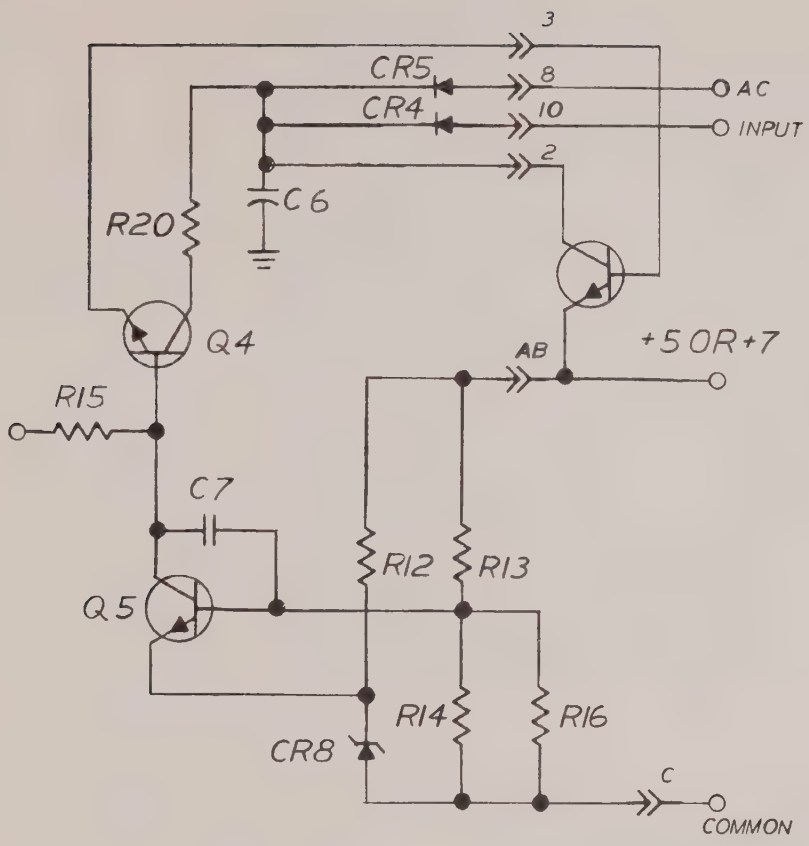


FIGURE 4

4.6 +1.4 and +2.1 Volt Reference Source

The +7 volt regulated power supplies of Models D500711-1, and -2 furnish current to a diode voltage divider consisting of CR9, CR10, and CR11. A nominal 1.4 volt reference is taken across CR10 and CR11. Capacitor C9 is used to filter this voltage. The combined voltage drop across CR9, CR10, and CR11 is used to furnish a nominal 2.1V reference.

5. DRAWINGS

D500711
C200188
C200210
C200349
B200409
C200476
C200505

REVISIONS					
NO SYM	DESCRIPTION	DATE	BY	CHK	APPD
J	REDRAWN, ADD SHEET 2, ADD DASH 2	23 OCT 1969	AG	GW	GS
K	REV PER ACO 2065	2 JAN 69	AG	GW	GS
L	ADD -6	12/4/69	SHAW	GW	GS
M	REV PER ACO 3016	12/16/69	AG	SHAW	GS
N	REV PER ACO 3005	1/2/70	SHAW	GW	GS
P	ADD -7 AND SHEET 3	2-26-70	SHAW	GW	GS
R	REV PER ACO 3077	7 APR 70	SHAW	GW	GS

NOTES

1. VALUES OF R7 R11 & R16 TO BE DETERMINED AT TIME OF ASSY OF -1
2. VALUES OF R11 & R16 TO BE DETERMINED AT TIME OF ASSY OF -2 -3 & -6
3. VALUE OF R7 TO BE DETERMINED AT TIME OF ASSY OF -4.
4. VALUE OF R16 TO BE DETERMINED AT TIME OF ASSY OF -5 & -7

ITEM	REF DESIGNATION
9	CR2, CR3, CR4, CR5, CR9, CR10, CR11
13	CR2, CR3, CR4, CR5

2	0	0	0	0	0	0		900-0730	58	TRANSISTOR		Q4 THRU Q8	
1	0	0	0	0	0	0		201-1101	57	RESISTOR, 1.1K, 1/2W, 5%		R12	
REF	0	0	0	0	0	0		C200527	56	SCHEMATIC			
1	0	1	0	0	0	0		201-2209	55	RESISTOR 22K 1/2W 5%		R20	
0	REF	0	0	0	0	0		C200505	54	SCHEMATIC			
0	0	AR	0	0	0	0		B50004-20	53	TUBING, TEFLON		NATURAL	
AR	AR	AR	0	0	0	0		307-0211	52	WIRE BUS SOLID #20		WHT	
0	0	1	0	0	0	0		201-1002	51	RESISTOR 10K 1/2W 5%		R10	
0	0	1	0	0	0	0		201-1000	50	RESISTOR 100Ω 1/2W 5%		R13	
0	0	1	0	0	0	0		66-8251	49	RESISTOR 6.65K 1/4W 1%		R5	
1	0	1	0	0	0	0		9348-0100	48	CAPACITOR 10PF +/- 1%		C8	
1	0	1	0	0	0	0		301-8203	47	CAPACITOR .02 μf		C7	
2	2	2	0	0	0	0		3483-0009	46	CAPACITOR 750 μf, 25V		C6	
0	0	2	0	0	0	0		9160-1449	45	TRANSISTOR		Q4 THRU Q8	
0	0	REF	0	0	0	0		C200476	44	SCHEMATIC			
0	0	0	REF	0	0	0		B2004-13	43	SCHEMATIC			
0	0	0	0	REF	0	0		C200*49	42	SCHEMATIC			
0	0	0	0	0	REF	0		C200210	41	SCHEMATIC			
0	0	0	0	0	0	REF		C200-88	40	SCHEMATIC			
QTY REQD -7	QTY REQD -6	QTY REQD -5	QTY REQD -4	QTY REQD -3	QTY REQD -2	QTY REQD -1	CODE IDENT NUMBER	PART OR IDENT NUMBER	ITEM	NOMENCLATURE OR DESCRIPTION		NOTES & REF DESIGNATIONS	

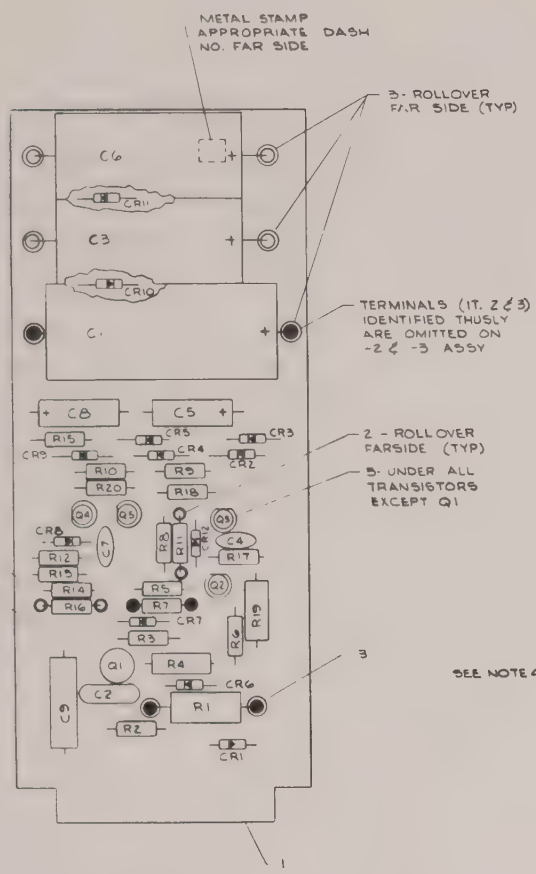
LIST OF MATERIALS

1	0	0	0	0	1	1		3317-9102	39	CAPACITOR .1 μf		C9	
0	0	0	0	1	1			3483-0009	38	750 μf, 25V		C6	
0	2	0	0	2	2	2		3348-0200	37	20 μf, 25V		C5, C8	
0	2	0	0	2	2	2		3403-9203	36	.02 μf		C4, C7	
1	1	1	0	1	1	1		3483-0008	35	250 μf, 60V		C3	
3	0	0	1	0	0	1		3406-9473	34	.047 μf		C2	
0	0	0	1	0	0	1		3358-0001	33	CAPACITOR 100 μf 150V		C1	
0	0	0	1	0	0	1		757-2201	32	RESISTOR 2.2K, 2W, 10%		R1	
3	1	0	0	1	1	1		202-1001	31	1K, 1W, 5%		R19	
3	1	0	0	1	1	1		201-2200	30	220Ω, 1/2W, 5%		R20	
0	1	0	0	1	1	0		201 3001	29	3K		R8	
3	1	0	0	1	1	0		201-3601	28	3.6K		R17	
1	1	1	0	0	1	1		201-1501	27	1.5K		R14	
0	0	0	0	1	0	0		201-5601	26	5.6K		R14	
0	1	0	0	1	0	0		201-4700	25	470Ω		R3	
2	0	0	0	0	2	2		201-4700	24	470Ω		R3, R5	
1	1	0	0	1	1	1		201-1502	23	15K		R10	
0	2	0	0	2	2	2		201-1101	22	1.1K		R9, R12	
0	1	0	0		1	1		201-2701	21	2.7K		R8	
0	0	0	0	0	0	1		20 1802	20	18K		R6	
0	0	0	1	0	0			201-1501	19	1.5		R5	
2	0	0	1	0	0	1		20 8201	18	8.2K 1/2W, 5%		R3	
1	0	0	1	0	0	1		202-4701	17	47K 1W 5%		R4	
0	0	0	0	1	0	1		206-5611	16	RESISTOR 1.5K 1/2W, 10%		R2	
0	1	0	0	1	1	1		B5000339	15	DIODE, IN461A		CR12	
0	1	0	0	1	0	0		801-0748	4	IN748A		CR8	
3	4	4	0	4	0	0		800-4384	13	IN4384		SEE TABLE	
0	0	0	1	0	0	1		R01-0750	2	N750A		CR6	
0	1	0	1	0	0	1		R01-0759	11	IN759A		CR7	
1	0	0	0	0	1	1		R0-0750	10	IN750A		CR8	
7	0	0	0	0	7	7		800-4384	9	IN4384		SEE TABLE	
0	0	0	1	0	0	1		800 4384	8	DIODE, IN4384		CR1	
0	4	0	0	4	4	4		900-0730	7	TRANSISTOR		Q2 THRU Q5	
0	0	0	1	0	0	1		900-0699	6	TRANSISTOR		Q1	
4	4	2	0	4	4	4		B2-0002	5	PAD, TRANSISTOR			
0	0	0	1	0	0	1		B2-0001	4	PAD, TRANSISTOR			
6	6	6	4	4	4	8		610-0013	3	TERMINAL, ROLLOVER			
2	4	2	2	4	4	6		310-0011	2	TERMINAL ROLLOVER			
1	1	1		1	1	1		C500-712	1	BOARD P.C.			
QTY REQ. -7	QTY REQ. -6	QTY REQ. -5	QTY REQ. -4	QTY REQ. -3	QTY REQ. -2	QTY REQ. -1	QTY REQD	CODE IDENT NUMBER	PART OR IDENT NUMBER	ITEM	NOMENCLATURE OR DESCRIPTION		NOTES & REF DESIGNATIONS

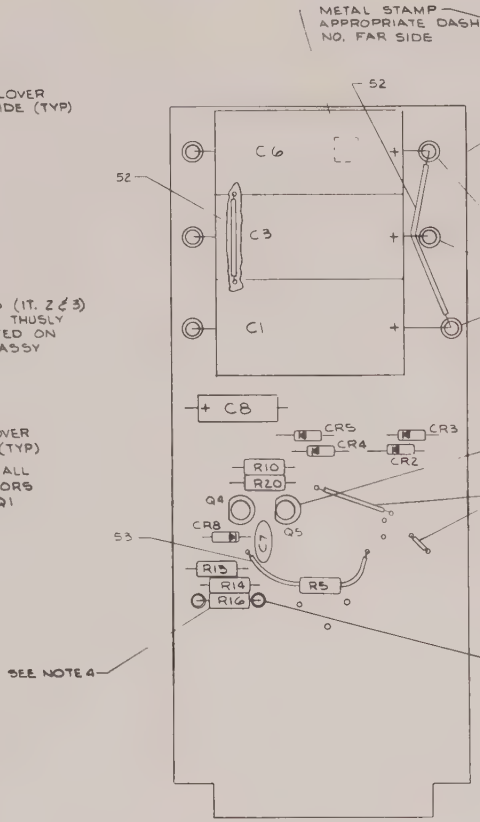
LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DRAWN 10-16-69 DATE	PULSE COMMUNICATIONS, INC. ALEXANDRIA, VA.	
TOLERANCES	CHECKED 11/12/69 DATE	BOARD, P.C. ASSY POWER SUPPLY	
2 PLACE DECIMALS ±	PROJ ENGRG DATE		
3 PLACE DECIMALS ±	PROD ENGRG DATE		
ANGLES ±			
DO NOT SCALE DRAWING			
MATERIAL		CODE IDENT NO 22818	SIZE D
FINISH		SCALE	SHEET 1 OF 3

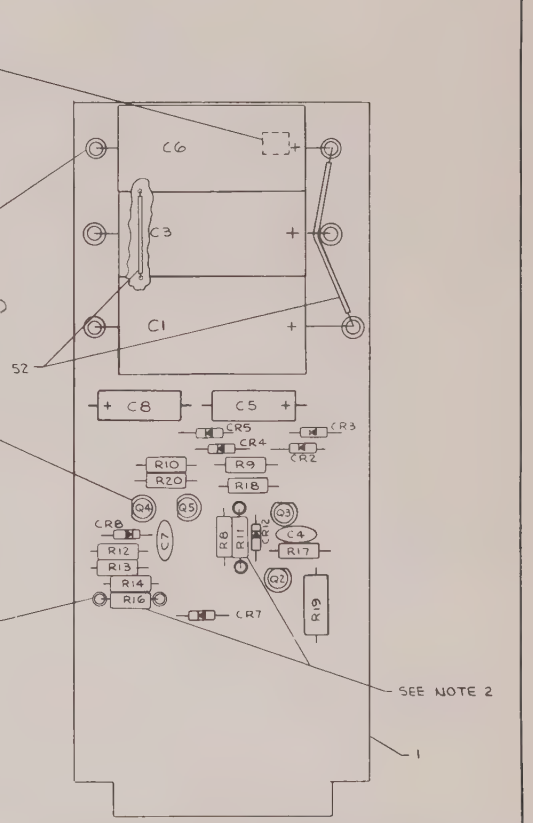
REVISIONS					
NO/SYM	DESCRIPTION	DATE	BY	CHK	APPD
J	REDRAWN; ADD SHEET 2, ADD DASH 5	7201 1969	AG	GL	GS
L	ADD -6	12/4/69	SHAW	L.L	FWE
M	REV PER ACO 3016	12/13/69	AG	SHAW	WG



-1 THRU -4



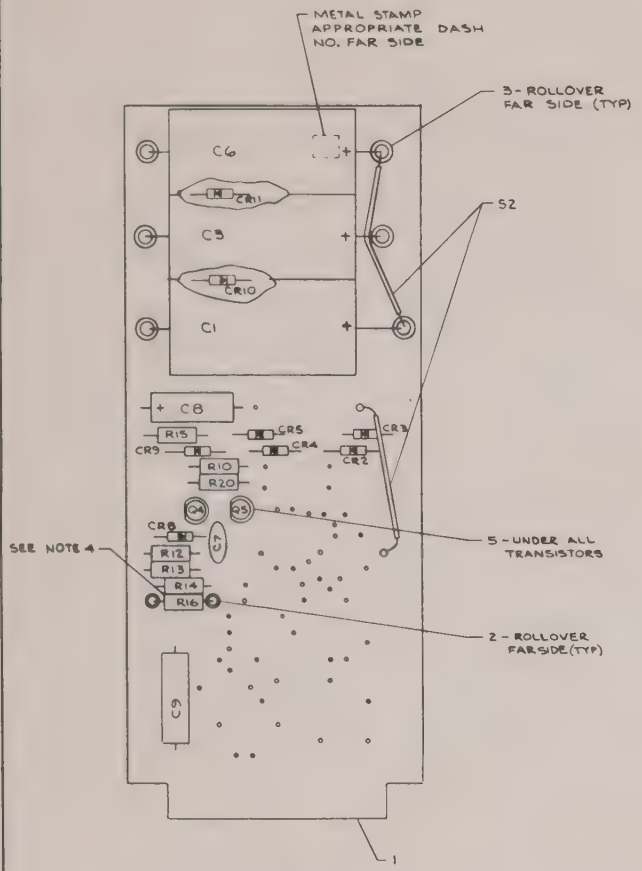
-5



-6

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	GREENE	10/17/69	PULSECOM PULSE COMMUNICATIONS, INC. ALEXANDRIA, VA.
TOLERANCES:	DRAWN	DATE	
2 PLACE DECIMALS ± .x	CHECKED	DATE	BOARD P.C. ASSY POWER SUPPLY
3 PLACE DECIMALS ± .xx	PROJ ENGRG	DATE	
ANGLES ±	PROD ENGRG	DATE	
DO NOT SCALE DRAWING	CAUTION: UNLESS THIS DRAWING BEARS THE NAMES OF THE PROJ ENGRG AND PROD ENGRG IT IS PRELIMINARY AND UNDER NO CIRCUMSTANCES IS TO BE USED FOR MANUFACTURING PURPOSES.		CODE IDENT NO 22818 SIZE D DRAWING NUMBER D500711
MATERIAL:	THIS DRAWING IS FURNISHED FOR ENGINEERING INFORMATION AND REFERENCE ONLY. THE FURNISHING OF THIS DRAWING DOES NOT CONVEY ANY LICENSE TO COPY OR REPRODUCE THE SAME.		SCALE 2/1 SHEET 2 OF 3
FINISH:			

REVISIONS					
NO/SYM	DESCRIPTION	DATE	BY	CHK	APPD



-7

QTY REQD -1	CODE IDENT NUMBER	PART OR IDENT NUMBER	ITEM	NOMENCLATURE OR DESCRIPTION	NOTES & REF DESIGNATIONS

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES:
2 PLACE DECIMALS ± ~
3 PLACE DECIMALS ± ~
ANGLES ± ~
DO NOT SCALE DRAWING
MATERIAL: ~
FINISH: ~

DRAWN: GREENE 1/27/70 DATE
CHECKED: [illegible] 1/27/70 DATE
PROJ ENGRG: DATE
PROD ENGRG: DATE

CAUTION: UNLESS THIS DRAWING BEARS THE VALUES OF MILITARY SPECS THE TOLERANCES IT IS PRESUMED SHOWN ARE THE MINIMUM ALLOWABLE IS TO BE USED FOR MANUFACTURING PURPOSES.

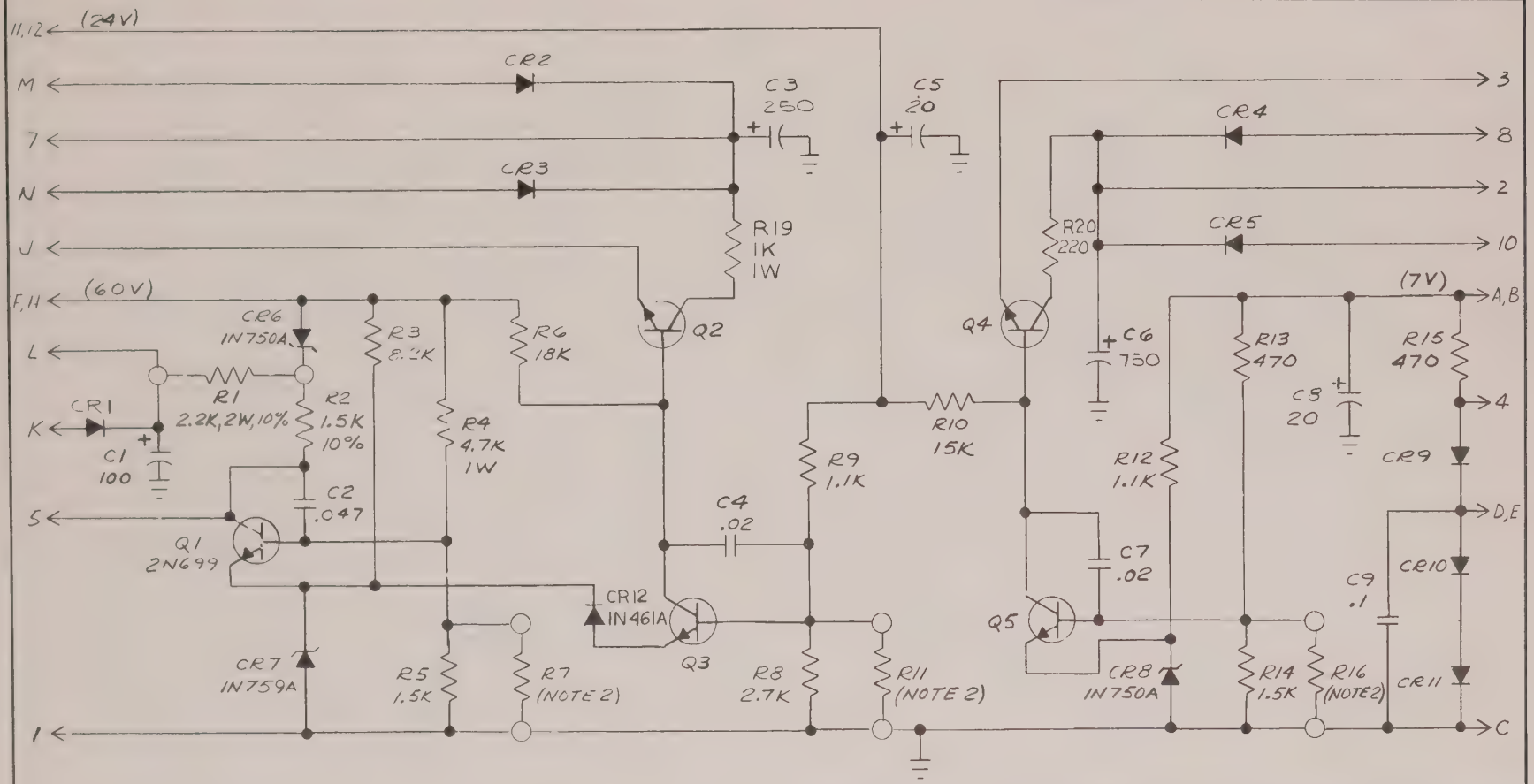
THIS DRAWING IS FURNISHED FOR PREPARING IN QUOTATIONS ONLY. ALL RIGHTS IN THE DESIGN OF THIS DRAWING DOES NOT CONVEY ANY REPRODUCTION OR MANUFACTURING RIGHTS.

PULSE COMMUNICATIONS, INC.
ALEXANDRIA, VA.

BOARD P.C. ASSY POWER SUPPLY

CODE IDENT NO: 22818
SIZE: D
DRAWING NUMBER: D500711
SCALE: 2/1
SHEET 3 OF 3

REVISIONS					
NO/SYM	DESCRIPTION	DATE	BY	CHK	APPD
A	REV PER ACO 1354	21 NOV 67	E.B.	J.C.	W.G.
B	REV PER ACO 1472	5 JAN 68	E.B.	W.G.	W.G.
C	REV PER CO 1818	14 MAY 68	RDC	W.G.	W.G.



NOTES

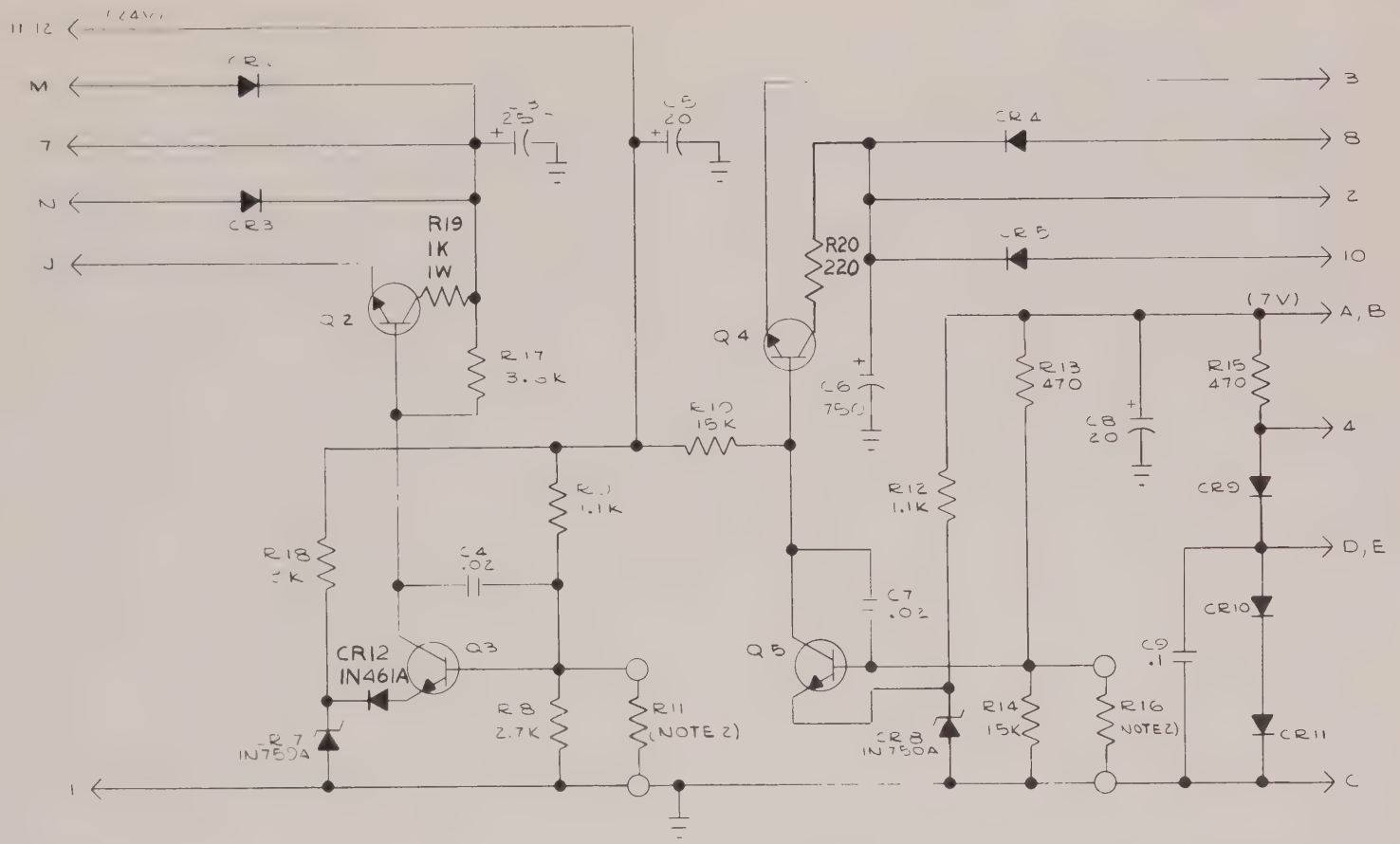
1- UNLESS SPECIFIED OTHERWISE :
- A) ALL RESISTANCE IN OHMS. ½ W, 5%
- B) ALL CAPACITANCE IN mf
- C) ALL DIODES TYPE IN4384
- D) ALL TRANSISTORS TYPE 2N730

2- VALUES OF R7, R11 & R16 ARE TO BE DETERMINED AT TIME OF ASSEMBLY

QTY REQD	CODE IDENT NUMBER	PART OR IDENT NUMBER	ITEM	NOMENCLATURE OR DESCRIPTION	NOTES & REF DESIGNATIONS
–1	LIST OF MATERIAL				

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DRAWN	17 May 67 DATE	PULSECOM PULSE COMMUNICATIONS, INC. ALEXANDRIA, VA.
TOLERANCES:	CHECKED	18 MAY 67 DATE	SCHEMATIC POWER SUPPLY (7V, 24V, & 60V)
2 PLACE DECIMALS ± ~	PROJ ENGRG	DATE	
3 PLACE DECIMALS ± ~	PROD ENGRG	6/20/68 DATE	
ANGLES ± ~			
DO NOT SCALE DRAWING			
MATERIAL: ~	CAUTION: UNLESS THIS DRAWING BEARS THE NAMES OF THE "PROJ ENGRG." "PROD ENGRG" IT IS PRELIMINARY AND UNDER NO CIRCUMSTANCES IS IT TO BE USED FOR MANUFACTURING PURPOSES.		CODE IDENT NO. 22818 SIZE C DRAWING NUMBER C200188
FINISH: ~	THIS DRAWING IS FURNISHED FOR ENGINEERING INFORMATION AND REFERENCE ONLY. THE FURNISHING OF THIS DRAWING DOES NOT CONVEY ANY RIGHTS OR LICENSE TO USE OR MANUFACTURING RIGHTS.		SCALE: ~ SHEET ~

REVISIONS					
NO. SYM	DESCRIPTION	DATE	BY	CHK	APPD
A	REV PER ACO 1472	[illegible]	E.B.	[illegible]	[illegible]
B	REV PER CO 1818	24.69	R&C	W.G.	W.G.



NOTES:

1- UNLESS SPECIFIED OTHERWISE:
   A) ALL RESISTANCE IN OHMS, 1/2W, 5%
   B) ALL CAPACITANCE IN μf
   C) ALL DIODES TYPE 1N4384
   D) ALL TRANSISTORS TYPE 2N730
2- VALUES OF R11, & R16 ARE TO BE DETERMINED AT TIME OF ASSEMBLY.

QTY REQD	CODE IDENT NUMBER	PART OR IDENT NUMBER	ITEM	NOMENCLATURE OR DESCRIPTION	NOTES & REF DESIGNATIONS
-1		LIST OF MATERIAL			

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TOLERANCES:
2 PLACE DECIMALS ± ~
3 PLACE DECIMALS ± ~
ANGLES ± ~
DO NOT SCALE DRAWING

MATERIAL: ~

FINISH: ~

T.E. BULL 7 NOV '67 DRAWN DATE

CHECKED DATE

PROJ ENGRG DATE

PROD ENGRG DATE

CAUTION: UNLESS THIS DRAWING BEARS THE NAMES OF THE "PROJ ENGRG." "PROD ENGRG." IT IS PRELIMINARY AND UNDER NO CIRCUMSTANCES IS IT TO BE USED FOR MANUFACTURING PURPOSES.

THIS DRAWING IS FURNISHED FOR ENGINEERING INFORMATION AND REFERENCE ONLY. THE FURNISHING OF THIS DRAWING DOES NOT CONVEY ANY REPRODUCTION OR MANUFACTURING RIGHTS

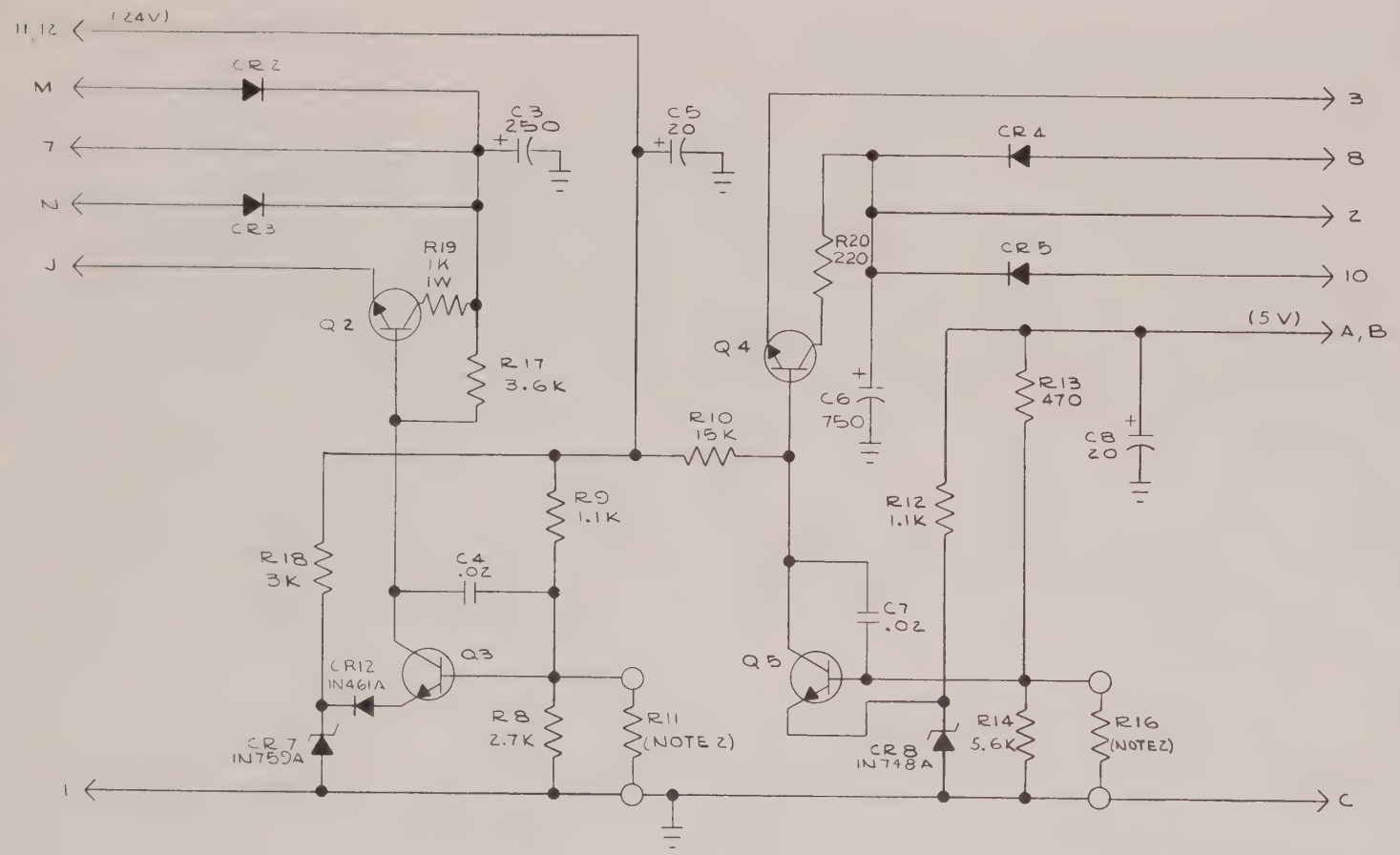
PULSECOM
PULSE COMMUNICATIONS, INC.
ALEXANDRIA, VA.

SCHEMATIC POWER SUPPLY (7V & 24V)

CODE IDENT NO.	SIZE	DRAWING NUMBER
22818	C	C200610

SCALE: ~ SHEET

REVISIONS					
NO/SYM	DESCRIPTION	DATE	BY	CHK	APPD
A	REV. PER CO. 1818	2 3 69	RdC	W.C.	W.G.



NOTES:

1- UNLESS SPECIFIED OTHERWISE:
- A) ALL RESISTANCE IN OHMS, 1/2W, 5%
- B) ALL CAPACITANCE IN mf
- C) ALL DIODES TYPE IN4384
- D) ALL TRANSISTORS TYPE 2N730

2- VALUES OF R11 & R16 ARE TO BE DETERMINED AT TIME OF ASSEMBLY.

QTY REQD	CODE IDENT NUMBER	PART OR IDENT NUMBER	ITEM	NOMENCLATURE OR DESCRIPTION	NOTES & REF DESIGNATIONS
-1		LIST OF MATERIAL			

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	W. GLEADALL DRAWN	9 DEC 68 DATE
TOLERANCES:	[illegible] CHECKED	11 DEC 68 DATE
2 PLACE DECIMALS ± ~	[illegible] PROJ ENGRG	11 DEC 68 DATE
3 PLACE DECIMALS ± ~	[illegible] PROD ENGRG	11 DEC 68 DATE
ANGLES ± ~		
DO NOT SCALE DRAWING		
MATERIAL: ~		
FINISH: ~		

PULSECOM — PULSE COMMUNICATIONS, INC. ALEXANDRIA, VA.

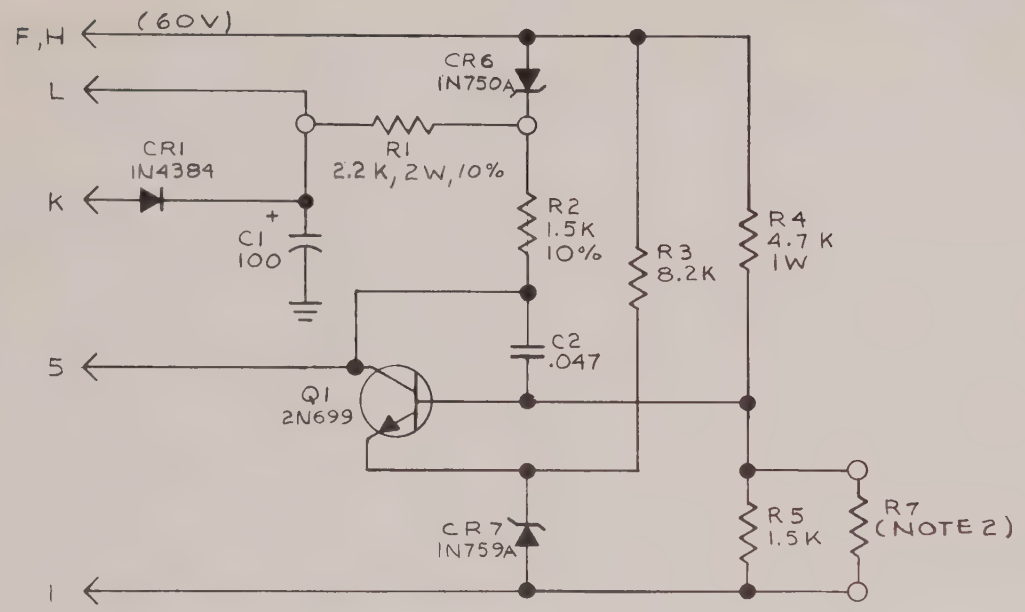
SCHEMATIC POWER SUPPLY (5V & 24V)

CODE IDENT NO. 22818 | SIZE C | DRAWING NUMBER C200349 | SCALE: ~ | SHEET

CAUTION: UNLESS THIS DRAWING BEARS THE NAMES OF THE "PROJ ENGRG." "PROD ENGRG" IT IS PRELIMINARY AND UNDER NO CIRCUMSTANCES IS IT TO BE USED FOR MANUFACTURING PURPOSES.

THIS DRAWING IS FURNISHED FOR ENGINEERING INFORMATION AND REFERENCE ONLY. THE FURNISHING OF THIS DRAWING DOES NOT CONVEY ANY REPRODUCTION OR MANUFACTURING RIGHTS.

REVISIONS					
NO/SYM	DESCRIPTION	DATE	BY	CHK	APPD



NOTES

1. UNLESS OTHERWISE SPECIFIED:
   A) ALL RESISTANCE IN OHMS, ½W, 5%.
   B) ALL CAPACITANCE IN μf.
2. VALUE OF R7 TO BE DETERMINED AT TIME OF ASSEMBLY.

QTY REQD — 1	CODE IDENT NUMBER	PART OR IDENT NUMBER	ITEM	NOMENCLATURE OR DESCRIPTION	NOTES & REF DESIGNATIONS

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	R d C	6-3-69 DATE
TOLERANCES:	DRAWN	
2 PLACE DECIMALS ±	S Buell	6-7-69 DATE
3 PLACE DECIMALS ±	CHECKED	
ANGLES ±	S Buell	6-7-69 DATE
DO NOT SCALE DRAWING	PROJ ENGRG	
MATERIAL:	H Stanley (S. Buell	6-3-69 DATE
FINISH:	PROD ENGRG	

CAUTION: UNLESS THIS DRAWING BEARS THE NAMES OF THE "PROJ ENGRG." "PROD ENGRG" IT IS PRELIMINARY AND UNDER NO CIRCUMSTANCES IS IT TO BE USED FOR MANUFACTURING PURPOSES.

THIS DRAWING IS FURNISHED FOR ENGINEERING INFORMATION AND REFERENCE ONLY. THE FURNISHING OF THIS DRAWING DOES NOT CONVEY ANY REPRODUCTION OR MANUFACTURING RIGHTS.

PULSECOM

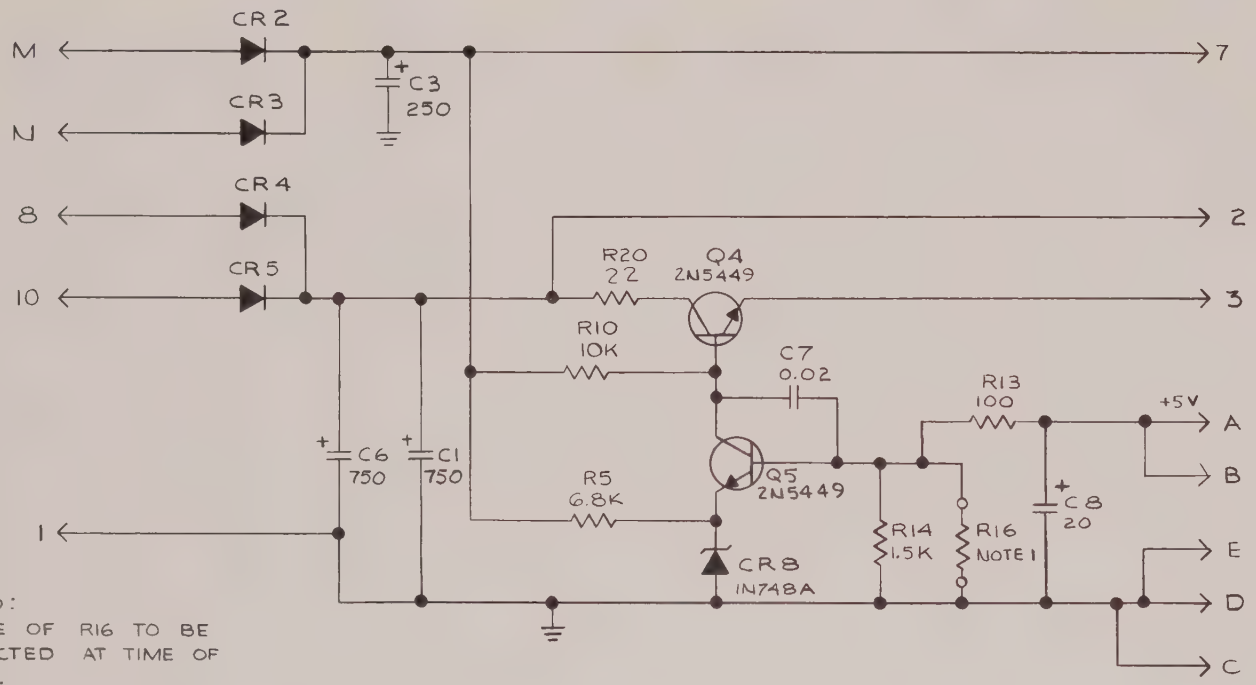
PULSE COMMUNICATIONS, INC.
ALEXANDRIA, VA.

SCHEMATIC
POWER SUPPLY

CODE IDENT NO.	SIZE	DRAWING NUMBER
22818	B	B200409
SCALE:		SHEET

DIETZGEN 1984 Ageproof Tracing Paper 80000

REVISIONS					
NO/SYM	DESCRIPTION	DATE	BY	CHK	APPD
A	REV PER 3005	1-2-70	SHAW	W.G.	W.G



NOTES:

1. VALUE OF R16 TO BE SELECTED AT TIME OF TEST.
2. UNLESS OTHERWISE SPEC.
   A. ALL RESISISTORS ARE IN OHMS 1/2W, 5 %.
   B. ALL DIODES ARE IN4384.
   C. ALL CAPACITORS ARE IN uf.

QTY REQD -1	CODE IDENT NUMBER	PART OR IDENT NUMBER	ITEM	NOMENCLATURE OR DESCRIPTION	NOTES & REF DESIGNATIONS
LIST OF MATERIAL					

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DRAWN	10-16-69 DATE
TOLERANCES:	CHECKED P.W. EBERSBERGER	17 OCT 69 DATE
2 PLACE DECIMALS ±	PROJ ENGRG P.W. EBERSBERGER	22 OCT 69 DATE
3 PLACE DECIMALS ±	PROD ENGRG	10/22/69 DATE
ANGLES ±		
DO NOT SCALE DRAWING		

PULSECOM — PULSE COMMUNICATIONS, INC. ALEXANDRIA, VA.

SCHEMATIC POWER SUPPLY TRANSLATOR (MODEL 1723-1)

DASH NO	NEXT ASSY.	USED ON
	APPLICATION	
1	D500711-5	1723-1

MATERIAL:

FINISH:

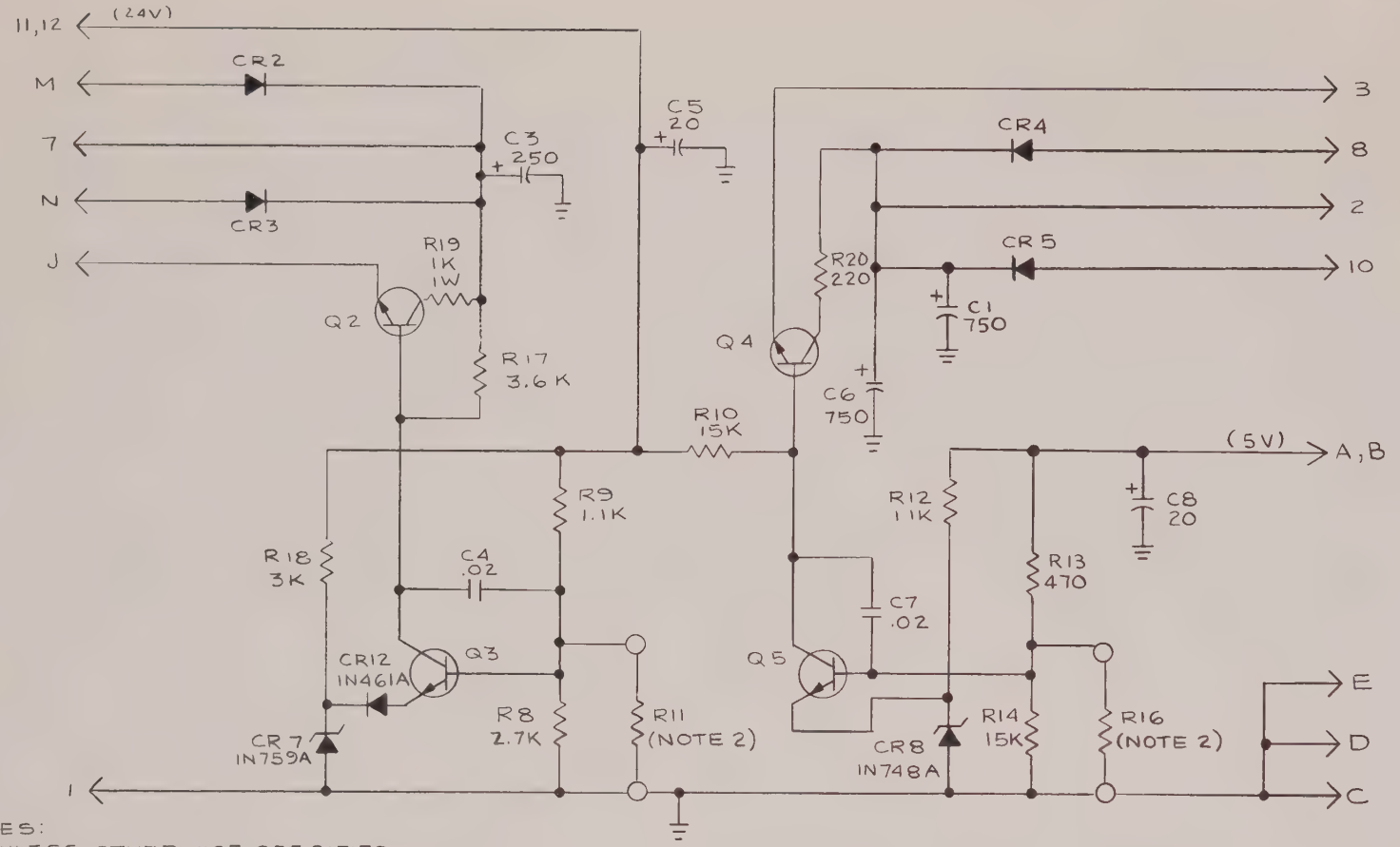
CAUTION: UNLESS THIS DRAWING BEARS THE NAMES OF THE "PROJ ENGRG." "PROD ENGRG" IT IS PRELIMINARY AND UNDER NO CIRCUMSTANCES IS IT TO BE USED FOR MANUFACTURING PURPOSES

THIS DRAWING IS FURNISHED FOR ENGINEERING INFORMATION AND REFERENCE ONLY THE PUBLISHING OF THIS DRAWING DOES NOT CONVEY ANY REPRODUCTION OR MANUFACTURING RIGHTS.

CODE IDENT NO.	SIZE	DRAWING NUMBER
22818	C	C200476

SCALE: — SHEET

REVISIONS					
NO/SYM	DESCRIPTION	DATE	BY	CHK	APPD
A	REV PER ACO 3016	13DEC69	A.G.	SHAW	W.G.



NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   A - ALL RESISTORS ARE IN OHMS, 1/2W, 5%.
   B - ALL CAPACITORS ARE IN μf.
   C - ALL DIODES ARE IN4384.
   D - ALL TRANSISTORS ARE 2N730.
2. VALUES OF R11 & R16 TO BE DETERMINED AT TIME OF ASSEMBLY

DASH NO.	NEXT ASSY.	USED ON
	D500711-6	

APPLICATION

QTY REQD -1	CODE IDENT NUMBER	PART OR IDENT NUMBER	ITEM	NOMENCLATURE OR DESCRIPTION	NOTES & REF DESIGNATIONS

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES:
2 PLACE DECIMALS ± ~
3 PLACE DECIMALS ± ~
ANGLES ± ~
DO NOT SCALE DRAWING
MATERIAL: ~
FINISH: ~

DRAWN Greene 12-9-69
G. LAYNE 12/9/69
CHECKED
P.W. EBERSBERGER 10 DEC 69
PROJ ENGRG
PROD ENGRG
DATE

CAUTION: UNLESS THIS DRAWING BEARS THE NAMES OF THE "PROJ ENGRG." "PROD ENGRG" IT IS PRELIMINARY AND UNDER NO CIRCUMSTANCES IS IT TO BE USED FOR MANUFACTURING PURPOSES.

THIS DRAWING IS FURNISHED FOR ENGINEERING INFORMATION AND REFERENCE ONLY. THE FURNISHING OF THIS DRAWING DOES NOT CONVEY ANY REPRODUCTION OR MANUFACTURING RIGHTS.

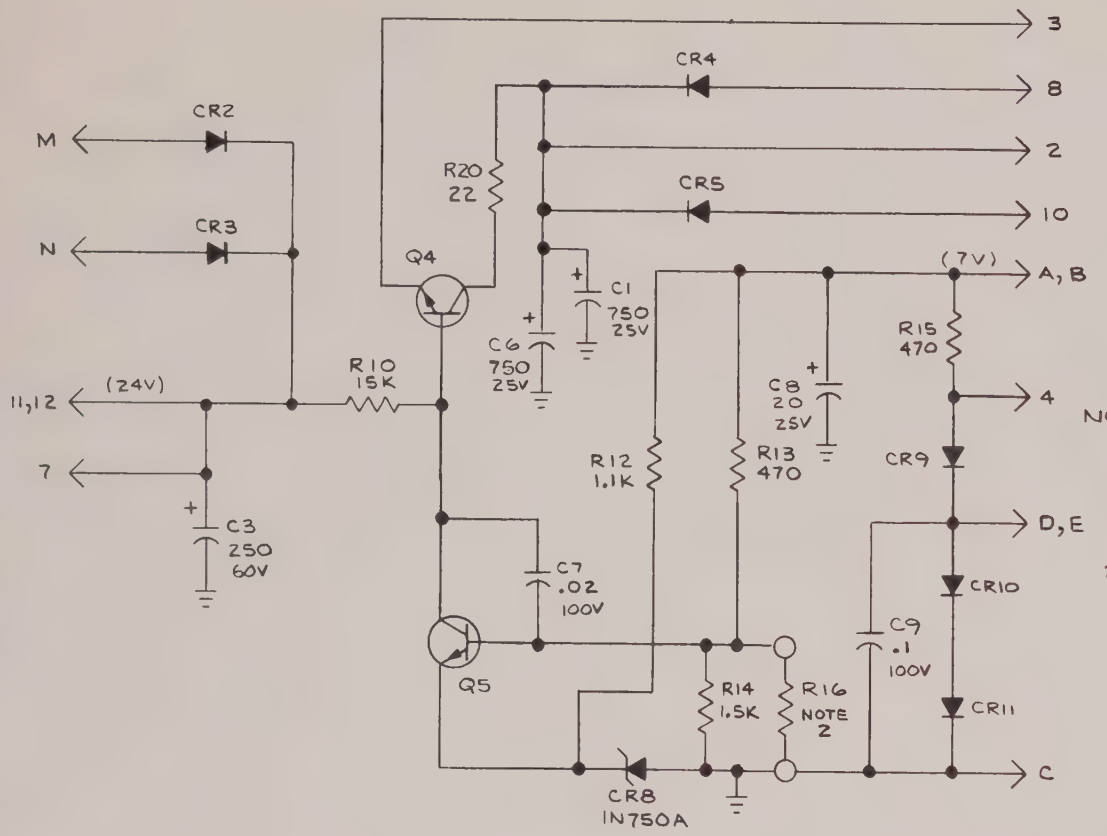
PULSECOM
PULSE COMMUNICATIONS, INC.
ALEXANDRIA, VA.

SCHEMATIC POWER SUPPLY (5 V & 24 V)

CODE IDENT NO.	SIZE	DRAWING NUMBER
22818	C	C200505

SCALE: ~ SHEET

REVISIONS					
NO/SYM	DESCRIPTION	DATE	BY	CHK	APPD



NOTES:
1- UNLESS OTHERWISE SPECIFIED:
A) ALL RESISTORS IN OHMS, 1/2 W, 5%
B) ALL CAPACITORS IN UF
C) ALL DIODES ARE IN4384
D) ALL TRANSISTORS ARE 2N730
2- VALUE OF R16 TO BE DETERMINED AT TIME OF ASSY

QTY REQD -1	CODE IDENT NUMBER	PART OR IDENT NUMBER	ITEM	NOMENCLATURE OR DESCRIPTION	NOTES & REF DESIGNATIONS
LIST OF MATERIAL					

7	D500711	
DASH NO	NEXT ASSY.	USED ON
APPLICATION		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES:
2 PLACE DECIMALS ± ~
3 PLACE DECIMALS ± ~
ANGLES ± ~
DO NOT SCALE DRAWING
MATERIAL: ~
FINISH: ~

W Marker 1-26-70 DRAWN DATE
P.W. EBERSBOKER 27 JAN 70 CHECKED DATE
P.W. EBERSBOKER 27 JAN 70 PROJ ENGRG DATE
QC 1/27/70 PROD ENGRG DATE
M. H. Jones 27 JAN 70

CAUTION: UNLESS THIS DRAWING BEARS THE NAMES OF THE "PROJ ENGRG." "PROD ENGRG" IT IS PRELIMINARY AND UNDER NO CIRCUMSTANCES IS IT TO BE USED FOR MANUFACTURING PURPOSES

THIS DRAWING IS FURNISHED FOR ENGINEERING INFORMATION AND REFERENCE ONLY. THE FURNISHING OF THIS DRAWING DOES NOT CONVEY ANY REPRODUCTION OR MANUFACTURING RIGHTS.

PULSECOM PULSE COMMUNICATIONS, INC. ALEXANDRIA, VA.

SCHEMATIC POWER SUPPLY (7V & 1.4V)

CODE IDENT NO.	SIZE	DRAWING NUMBER
22818	C	C200527
SCALE: ~		SHEET

INSTRUCTION MANUAL

EIA Interface
Model C100452
Issue 1

IN#186
(11/69)

CONTENTS

1. GENERAL

2. SPECIFICATIONS

3. CIRCUIT DESCRIPTION

C100452 Drawing

C200372 Drawing

INSTRUCTION MANUAL

EIA INTERFACE
Model C100452

1. GENERAL

The PULSECOM Model C100452 EIA Interface has been designed to translate EIA voltage mode signals to a form usable by standard PULSECOM Solid State Selectors. The interface board will also translate transmitter-distributor and answerback signals to the EIA level. The board has a self-contained power supply to drive the EIA output.

2. SPECIFICATIONS

Input signal	+3 v dc to +25 v dc spacing. -3 v dc to -25 v dc marking.
Output signal	+16 v dc spacing, -16 v dc marking-nominal
Power supply requirements	Unregulated ac input from selector. +1.4 v dc reference, +7 v dc.

3. CIRCUIT DESCRIPTION

The circuits contained on the Model C100452 EIA Interface board are shown on Schematic Drawing C200372. There are three types of circuits on this board: a power supply, input-output voltage translators, and drivers. They will be described in order.

3.1 Power Supply — The plus and minus 16 volt dc power supply is formed by diodes CR1 and CR2, along with filter capacitor C1 to furnish +16 v dc unregulated. The negative portion of the sine wave is rectified by diode CR2 and filtered by capacitor C2 to furnish -16 v dc unregulated. These voltages are used to drive the EIA output.

3.2 Voltage Translators — There are two voltage translators, one for input signals and one for output signals.

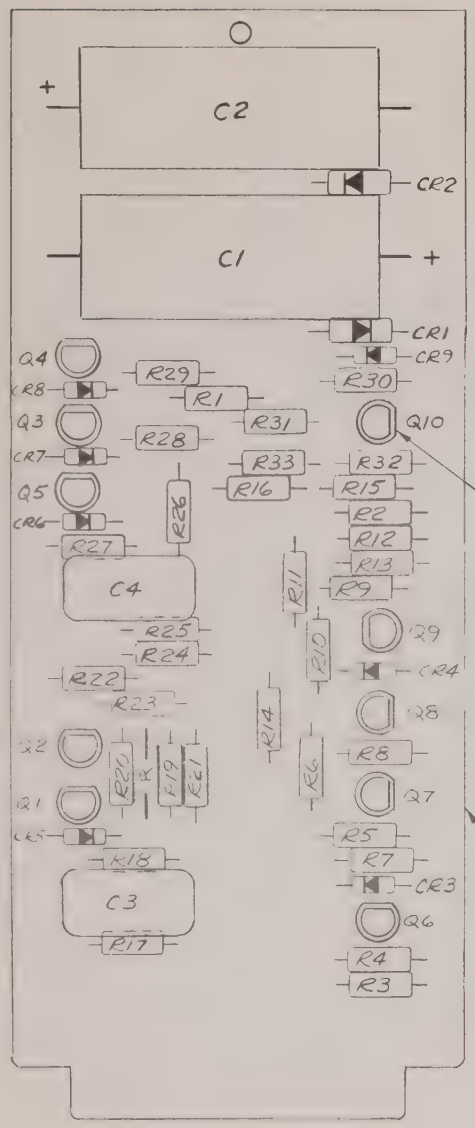
Input signals are translated by transistors Q1 and Q2. The EIA input signals appear on pin A. They are fed through R17 and R18 to the base of Q1. When the input signal goes negative, transistor Q1 will turn off, placing a positive signal on pin 2, the signal to the selector. In this

state, transistor Q2 will be turned on, removing the positive bias from the base of Q2. This makes a sharp turn off of Q1. When the input signal goes positive, transistor Q1 will turn on, placing the reference on output pin 2, and turning Q2 off. Turning Q2 off restores the positive bias to the base of Q1, making the turn on sharp. Diode CR5 prevents excessive reverse emitter-base bias on Q1. Capacitor C3 prevents noise spikes from giving a false signal.

Output signals are set to EIA levels by transistors Q6, Q7, and Q8. Signals that are to be transmitted appear on pin 11. The signals at pin 11 are used to turn transistor Q6 on and off. When pin 11 is high or open, transistor Q6 will be turned off. This places - 16 v on the bases of transistors Q7 and Q8, which are connected as complementary emitter followers. With -16 v at their bases, Q7 will be off and Q8 will be on to apply -16 v to output pin M through resistor R6. When pin 11 is low, transistor Q6 will be turned on, placing +16 v on the bases of Q7 and Q8. This will turn Q8 off and Q7 on to apply +16 v to output pin M through resistor R6.

3.3 Drivers — Transistors Q9 and Q10 are connected as independent auxiliary drivers to switch the EIA output as required. Transistors Q3, Q4, and Q5 are used to switch a line to reference.

REVISIONS					
NO/SYM	DESCRIPTION	DATE	BY	CHK	APPD
A	REV PER ACO 2090	12-18-69	RAC	W.C	W.C



10-UND ALL TRANSISTOR

ITEM	REF DESIGNATION
8	Q6, Q8, Q9, Q10
9	Q1 TO Q5 & Q7
13	R11, R14, R16, R33
15	R12, R13, R15, R26, R32
16	R17, R18, R25, R28, R29
18	R4, R7, R9, R19, R22, R30

NOTE:
1. EITHER 801-0461 OR B500034 MAY BE USED.

QTY REQD --1	CODE IDENT NUMBER	PART OR IDENT NUMBER	ITEM	NOMENCLATURE OR DESCRIPTION	NOTES & REF DESIGNATIONS
3		201-2202	19	RESISTOR 22K, 1/2W, 5%	R3, R10, R31
6		201-1002	18	10K,	SEE TABLE
3		201-4701	17	4.7K,	R21, R23 & R27
5		201-3301	16	3.3K,	SEE TABLE
5		201-2201	15	2.2K,	SEE TABLE
1		201-1501	14	1.5K,	R24
4		201-3300	13	330Ω,	SEE TABLE
3		201-4709	12	47Ω,	R5, R6, R8
2		201-2209	11	RESISTOR 22Ω, 1/2W, 5%	R1, R2
10		82-0002	10	PAD, TRANSISTOR	
1		900-5449	9	TRANSISTOR 2N5449	SEE TABLE
4		900-5447	8	TRANSISTOR 2N5447	SEE TABLE
7		SEE NOTE1	7	DIODE IN461A	CR3 TO CR9
2		800-4384	6	DIODE IN4384	CR1, CR2
2		3406-9102	5	CAPACITOR .1mf	C3, C4
1		201-1202	4	RESISTOR 12K, 1/2W, 5%	R20
2		3483-0009	3	CAPACITOR 750mf	C1, C2
REF		C200372	2	SCHEMATIC	
1		C501627	1	BOARD, P.C.	

LIST OF MATERIAL

DASH NO	NEXT ASSY.	USED ON
	APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES:
2 PLACE DECIMALS ± ~
3 PLACE DECIMALS ± ~
ANGLES ± ~
DO NOT SCALE DRAWING
MATERIAL: ~
FINISH: ~

DRAWN [illegible] DATE 9-29-69
CHECKED [illegible] DATE 9-30-69
PROJ ENGRG [illegible] DATE 10/1/69
PROD ENGRG [illegible] DATE 10/1/69

CAUTION: UNLESS THIS DRAWING BEARS THE NAMES OF THE "PROJ ENGRG." "PROD ENGRG" IT IS PRELIMINARY AND UNDER NO CIRCUMSTANCES IS IT TO BE USED FOR MANUFACTURING PURPOSES

THIS DRAWING IS FURNISHED FOR ENGINEERING INFORMATION AND REFERENCE ONLY. THE FURNISHING OF THIS DRAWING DOES NOT CONVEY ANY REPRODUCTION OR MANUFACTURING RIGHTS

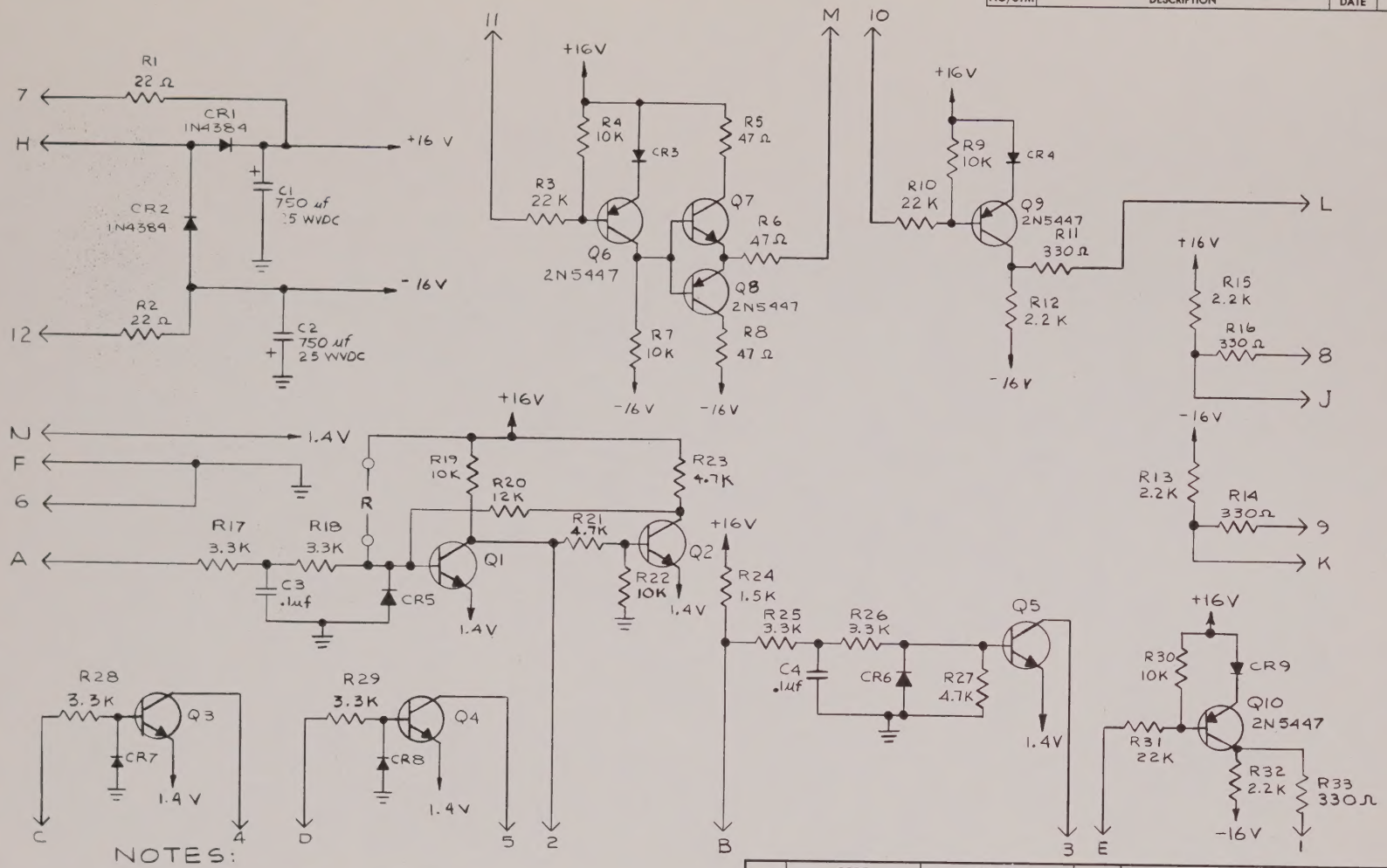
PULSECOM
PULSE COMMUNICATIONS, INC.
ALEXANDRIA, VA.

BOARD, P.C. ASSY E I A INTERFACE

CODE IDENT NO.	SIZE	DRAWING NUMBER
22818	C	C100452

SCALE: 2/1 SHEET

REVISIONS					
NO/SYM	DESCRIPTION	DATE	BY	CHK	APPD



NOTES:

1. UNLESS OTHERWISE SPECIFIED.
   A.) ALL DIODES ARE IN461A
   B.) ALL TRANSISTORS ARE 2N5449
   C.) ALL RESISTORS ARE IN OHMS
   ½ W 5%.

QTY REQD -1	CODE IDENT NUMBER	PART OR IDENT NUMBER	ITEM	NOMENCLATURE OR DESCRIPTION	NOTES & REF DESIGNATIONS
LIST OF MATERIAL					

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DRAWN R J C 2/27/69 DATE	PULSE COMMUNICATIONS, INC. ALEXANDRIA, VA.
TOLERANCES:	CHECKED P.W. EBERSBERGER 1 OCT 69 DATE	SCHEMATIC
2 PLACE DECIMALS ± —	PROJ ENGRG 10-4-69 DATE	EIA INTERFACE
3 PLACE DECIMALS ± —	PROD ENGRG 10/6/69 DATE	
ANGLES ± —		
DO NOT SCALE DRAWING	CAUTION: UNLESS THIS DRAWING BEARS THE NAMES OF THE "PROJ ENGRG." "PROD ENGRG" IT IS PRELIMINARY AND UNDER NO CIRCUMSTANCES IS IT TO BE USED FOR MANUFACTURING PURPOSES.	CODE IDENT NO. 22818 / SIZE C / DRAWING NUMBER C 200372
MATERIAL: —	THIS DRAWING IS FURNISHED FOR ENGINEERING INFORMATION AND REFERENCE ONLY. THE FURNISHING OF THIS DRAWING DOES NOT CONVEY ANY REPRODUCTION OR MANUFACTURING RIGHTS.	SCALE: — / SHEET
FINISH: —		

Electronic Services
Los Angeles
M14730X

PULSECOM